Configurable waveform and trigger generation Hardware and Software for 2D Air Surveillance Radar

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***Abstract* - The Waveform & Trigger Generation hardware and software is designed and developed for generation of programmable IF 30 MHz expanded pulse, wide-range of waveforms required for Radar operation and synchronization triggers for Receiver, Signal processor and Transmitter of 2D Air surveillance radar for L Band application. The Radar is operational on-board Indian Naval ships.**

***keywords* - Pulse compression, IF 30 MHz expanded pulse, LFM, co-efficient, Linux platform, firmware, Triggers, Radar Controller, Target simulation**

I. INTRODUCTION

The Radar referred in the present context is coherent Radar which provides a detection volume space up to 160 km in range, elevation coverage of 40° and 360° in bearing and presents video signals for display purpose as well as tracks for target track generation. The design is aimed at providing a high performance, technologically superior long range L-Band air surveillance Radar for installation and use on board large and medium size Naval ships and on-shore establishments.

Waveform & Trigger Generation card is the considered as heart of the state-of-the-art Radar system. The Waveform & Trig Gen PCB is designed with latest technology modules for generation of all the waveforms and triggers required for Radar operation with provision for configuration in real-time.

II. SALIENT FEATURES

Waveform & Trigger Gen card is state of the art design and is multifunctional module. Salient features of the module are provided below:

- Generation of IF chirp expanded pulse signal with LFM of 5 MHz bandwidth for 4us, 75us and 150us.
- Real-time trigger generation and synchronization with transmitter, receiver and signal processing modules to enable Radar operation
- Generation of gate pulse for activating Solid-state power amplified based transmitter
- Real-time acceptance of control commands from Radar controller and generation of appropriate chirp waveform and system triggers
- Generation of triggers to enable forward and reflected power measurements in real-time
- Generation of triggers required by signal generator instrument for calibrating complete receive chain.
- Simulation of targets to enable verification and validation of receive chain of the Radar
- Continuous monitoring of antenna heading line and bearing pulses and synchronization of for generation of pulses.
- Configurable sector blanking provision

III. HARDWARE DETAILS

The Waveform & Trigger Gen card is an indigenously developed board consisting of 12 layer PCB with Xilinx Virtex 5 FX series (XC5VFX70T-1FFG1136I) FPGA inclusive of Power PC hardcore IP. The board comprises of hardware interfaces such as Gigabit Ethernet, UART, Differential I/O for generating Triggers, TTL signal interface, 32 MB NOR flash and 128 MB DDR2 SDRAM.

The hardware also consists of 16 bit ADC with eight channels multiplexer for monitoring analog signals, four channels 14 bit DAC with 40 Msps speed for generation of arbitrary analog waveform over SMA, Two channel 14 bit DAC with 160 Msps speed for generation of IF of 30 MHz expanded chirp waveform using 400 MHz external sampling clock on SMA. Hardware is also embedded with 100 MHz oscillator and Eight channel 16-bit ADC with sampling rate of 1 Msps.

The board is powered from single 5V power input from backplane connector. The board is standard double euro size with a front fascia.

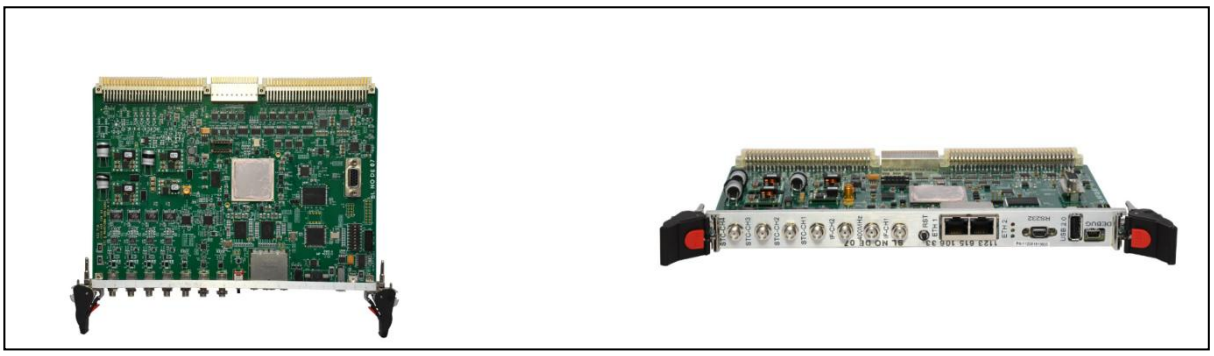

Fig 1. WTG Hardware

IV. SOFTWARE DETAILS

Software/Firmware comprises of VHDL and C programs. Waveform and trigger generation in real-time for various configurable Radar operation modes is done through VHDL programming using XILINX ISE.

Software Development Kit (SDK) is installed on Linux platform for development C program based firmware which runs of Power PC. Upon compilation the SDK generates four binary images by name u-boot.bin, uImage, virtex440-ml507.dtb and uramdisk.image which consists embedded OS image, kernel level driver related configurations, pin configurations and user application. These binary images are flashed to the hardware using XILINX ISE to enable firmware interface with VHDL.

The firmware communicates with the Radar Controller through Ethernet UDP interface to receive control commands in real-time, validates and forwards the pulse width and PRT related details to RTL logic for appropriate waveform and trigger generation and modification of pulse chirp as intended for Radar operation. The firmware also computes the sector width and centre and forwards the same to RTL logic for performing sector blanking operations.

The RTL logic in VHDL generates all the system triggers and chirp waveform with reference to 400 MHz clock and antenna heading line. RTL logic also receives heading line and bearing from Antenna which is further used by C program for computing current position of antenna and transmission of the same to other Radar subsystems via UDP in real-time at 10ms rate.

In addition to the above, the firmware, acknowledges the receipt of control command from Radar controller and also monitors and provides periodic status updates on chirp signal, PRT and pulse width characteristics, heading line and bearing on request from Radar controller.

V. IMPLEMENTATION

The Radar is designed for 5RPM and 10RPM modes of antenna rotation. RTL logic is synchronized with Antenna signal and 400 MHz clock is used as reference for generation of all system triggers and pulses required by transmitter, receiver and signal processing modules of the Radar system.

VHDL program generates LFM expanded pulse as required based on antenna rotation i.e. LFM of 4us (short pulse) followed by 150us (long pulse) is generated when antenna rotation is 5RPM where as LFM of 4us (short pulse) followed by 75us (long pulse) is generated when antenna rotation is 10RPM. The PRT combination varies based on staggered or non-staggered PRF selection and is generated in real-time respectively for both RPMs based on the control command received from Radar Controller

The functional blocks of the PCB are DDS core, ROM, Band pass Filter and scalar modules. Mathematical algorithm is used to find the co-efficient of expanded chirp pulse and those values are stored in ROM blocks and Soft filter is used for removal of harmonics. The functional blocks required for chirp generation are designed using MATLAB Simulink tool.

Pulse expanded chirp signal of 4us, 75us and 150us is generated with LFM at 5 MHz bandwidth. up chirp from 27.5 MHz to 32.5 MHz is been generated. Chirp signals are generated in real time, based on commands received from Radar Controller. For generating chirp, external 400 MHz clock is interfaced with FPGA. FPGA generates control signals and 14 data bits required for 160 Msps DAC. Two such DACs are interfaced for actual chirp generation and for simulated target signal generation.

Chirp signal generated by Waveform & Trig Gen PCB is captured and analyzed using Real-time Spectrum Analyzer instrument as shown in Fig 1 – 6. The expanded LFM pulse is compressed on reception to achieve the advantage of higher bandwidth and better target resolution as depicted in Fig 7.

Sector blanking is also configured in real-time through Radar Controller GUI for withdrawing triggers in a particular sector. Waveform & Trig Gen card also generates noise trigger to enable measurement of forward power and reflected power, and also generates trigger required for signal generator for calibrating the entire receive chain of the Radar system.

In addition to the above mentioned functionalities Waveform & Trig Gen card also simulates targets for verification and validation of entire receive chain of the Radar system. Simulation of stationary targets and the targets moving up to 3 mach speed have been implemented with option of Doppler variation.

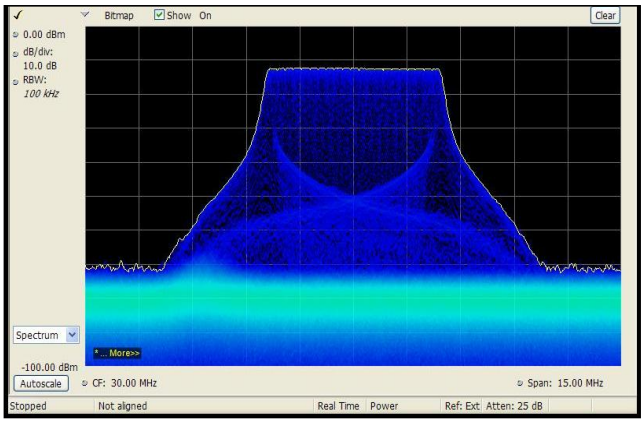

Fig 2. Frequency spectrum domain

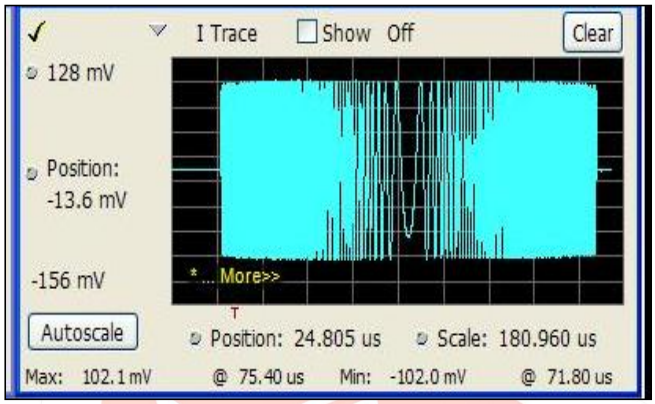

Fig 3. Chirp signal-time domain

Fig 4. Frequency v/s Time

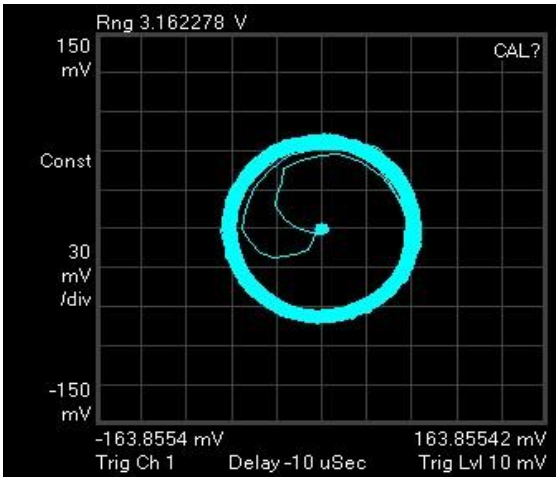

Fig 5. Chirp signal – 1 and Q plot

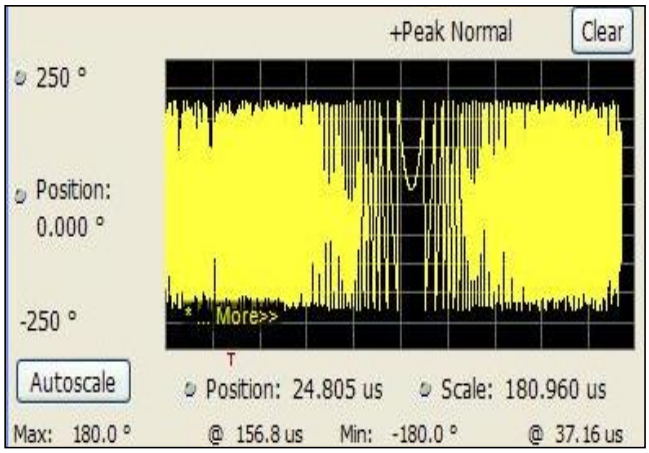

Fig. 6 Phase v/s Time

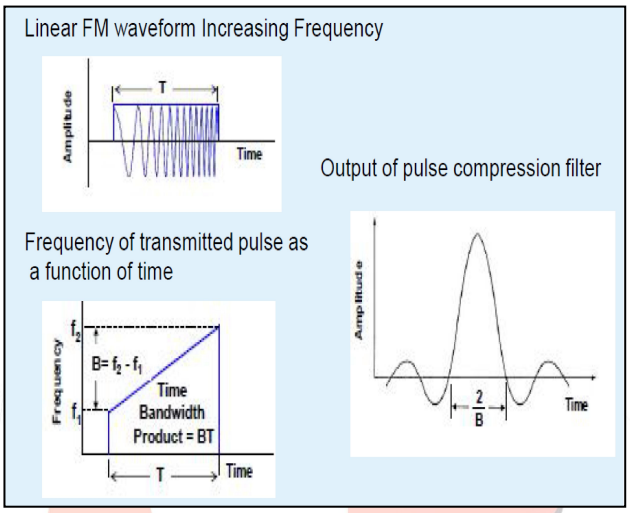

Fig 7. LFM expansion and compression

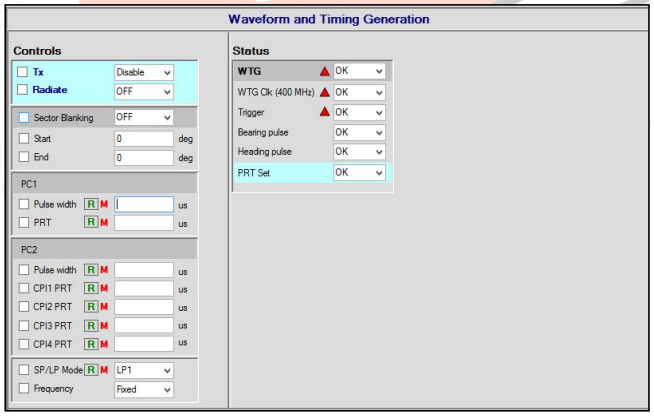

Fig 8. WTG parameters controlled by GUI

VI. CONCLUSION

This paper elaborates about indigenous design and development of a compact Waveform and Trigger Generation card for use in pulsed Radar, along with details of its functionalities, hardware, software, implementation methodology and test results. The card is operational in ship-mounted 2D air surveillance Radar designed and developed for Indian Navy. The generic architecture of Waveform & Trig Gen hardware and software enables its usage across various Radars with modification of LFM/NLFM co-efficients. In addition, the timing (i.e. pulse width and PRT) of triggers can be dynamically configured in real-time through UDP interfaced with GUI as required for application in different Radars.

VII. ACKNOWLEDGMENT

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