DX-MOCCII Based Voltage Mode First Order All Pass Filter

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Abstract - Here a new voltage mode first order all-pass filter is designed using a single DX-MOCCII. The circuit uses two resistors and one capacitor. Non-ideality analysis and sensitivity analysis is also performed here. The proposed circuit has low sensitivity. The theoretical results are verified through CADENCE ORCAD Pspice simulator with 0.25µm TSMC process parameter. The simulated results agree well with the theoretical predictions.

IndexTerms - All pass filter, DX-MOCCII, Voltage mode, Analog building block.

I. INTRODUCTION

In many analog signals processing application all-pass filter is one of the most important building block. It is also called phase shifter. Using this all pass filter there are many applications: communication system, instrumentation system, delay and equalization system, quadrature oscillators, band pass filter etc.

In literature there are numerous all-pass filters which are based on analog building block such as: current conveyors (CC) [1], second generation current conveyor (CCII) [2], third generation current conveyor (CCIII) [3], Second generation current-controlled current conveyor (CCCII) [4], inverting voltage buffer (IVB) [5], Extra-X current controlled conveyor (EX-CCII) [6], operational transconductance amplifier (OTA) [7], differential voltage current conveyor (DVCC) [8], differential difference current conveyor (DDCC) [9], dual-X second generation current conveyor (DXCCII) [10], differential difference dual-X second generation current conveyor (DD-DXCCII) [11], fully differential second generation current conveyor (FDCCII) [12], current differencing buffered amplifier (CDBA) [13], universal voltage conveyor (UVC) [14], voltage differencing inverting buffered amplifier (VDIBA) [15], current controlled conveyor transconductance amplifier (CCCTA) [16] have been reported.

Here a new DX-MOCCII based voltage mode APF is presented. The proposed circuit uses two resistors and one capacitor. The circuit is simulated through CADENCE ORCAD Pspice simulator.

II. DX-MOCCII BUILDING BLOCK

The basic building block and CMOS circuit diagram of DX-MOCCII is shown in Fig.1 and Fig.2 respectively. In this block diagram Xp,Xn are the non-inverting and inverting terminal to process the signal to the Zp and the Zn terminal respectively.

Fig.1: Block diagram of DX-MOCCII
The terminal current and voltages of the DX-MOCCII is related as follows:

\[ \begin{align*}
& I_y = 0 \\
& V_{xp} = V_y, \quad V_{xn} = -V_y \\
& I_{zp} = I_{xp}, \quad I_{zn} = I_{xn}
\end{align*} \tag{1} \]

Where \( x_p, x_n, y \) are the input terminals and \( z_p, z_n \) are the output terminals of DX-MOCCII, \( y \) terminal’s current is zero and \( x_p \) and \( x_n \) terminals currents are conveyed to the \( z_p \) and \( z_n \) terminal, \( x_p \) terminals voltage is equal to the \( y \) terminals voltage and \( x_n \) terminals voltage is equal to the \(-\)ve of \( y \) terminals voltage.

### III. PROPOSED ALL-PASS FILTER CIRCUIT

DX-MOCCII based voltage mode all pass filter circuit is shown in Fig.3. Transfer function of the proposed circuit can be obtained by using the circuit and the port relationship of DX-MOCCII.

\[ \frac{V_{out}}{V_{in}} = \frac{1-sCR_2}{1+sCR_1} \tag{2} \]

Phase response of the proposed circuit is given by

\[ \phi(\omega) = -2\tan^{-1}(\omega RC) \tag{3} \]

Here pole frequency is given by

\[ \omega_p = \frac{1}{RC} \tag{4} \]

Sensitivity of the proposed all-pass filter circuit w.r.t various components can be expressed as:

\[ S_{R_2} = -1, S_C = 0 \tag{5} \]

Sensitivity of the pole frequency \( \omega_p \) are small and its maximum value is -1

### IV. NON-IDEAL ANALYSIS OF THE PROPOSED CIRCUIT

Non-ideality analysis can be obtained in two ways: (1) due to transfer gain and (2) due to parasite effects.

#### 1.1. Non-ideality due to transfer gain:

The matrix equation due to non ideal characteristics can be expressed as:
\[
\begin{bmatrix}
I_y \\
V_{xp} \\
V_{xn} \\
I_{zp} \\
I_{zn}
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
\beta_p & 0 & 0 \\
-\beta_n & 0 & 0 \\
0 & \alpha_p & 0 \\
0 & 0 & \alpha_n
\end{bmatrix}
\begin{bmatrix}
V_y \\
V_{xp} \\
V_{xn}
\end{bmatrix}
\] (6)

Here \(\beta_p, \beta_n\) are voltage transfer gain of \(X_p\) and \(X_n\) port respectively. \(\alpha_p, \alpha_n\) are current gain from \(X_p\) and \(X_n\) port to \(Z_p\) and \(Z_n\) port respectively.

The modified equation for series inductor can be written as:

\[
\frac{V_{out}}{V_{in}} = \frac{\alpha_p - s CR_2}{1 + s CR_1}
\] (7)

1.2. Parasitic component non-ideality:

The parasitic model of DX-CCII is shown in Fig.4. Here \(R_y, R_{zp}, R_{zn}\) have high parasitic resistance value and is attached with \(Y, Z_p, Z_n\) port respectively. \(R_{xp}, R_{xn}\) are low parasitic resistance connected in series with \(X_p, X_n\) terminals. \(C_{xp}, C_{xn}\) parasitic capacitance has very low value connected in \(X_p, X_n\) terminals.

Transfer function obtained using the above approximation is

\[
\frac{V_{out}}{V_{in}} = \left( \frac{C}{C + C_{zn}} \right) \left( \frac{s - 1/C R_{equ}}{s + 1/R (C + C_{zn})} \right)
\] (8)

Where, \(R_{equ}' = R_{zp} + R_{xn}\) and \(R' = R / R_{mn}\)

V. SIMULATION RESULTS

Here the proposed circuit is simulated by PSPICE simulator using 0.25\( \mu \)m TSMC level-3 technology parameter. \(V_{DD}\) and \(V_{SS}\) are taken as \/+1.25\( V\) and bias voltage taken -0.3\( V\). The aspect ratio of various MOSFET transistor of DX-MOCCII is given in Table-1. To design the proposed all-pass filter capacitor and resistor values are taken 45\( \mu \)F, 1.5\( K\)\( \Omega\), 3\( K\)\( \Omega\) respectively with a pole frequency 2.36MHz. The gain and phase response of the proposed circuit is shown in Fig.5 and the transient response is also shown in Fig.6. Frequency spectrum of the input and output signal is shown in Fig.7. 90\( ^\circ\) phase shift between the input and output signal is shown in Fig.8 which confirms the quadrature relationship between input output waveform.

<table>
<thead>
<tr>
<th>Transistors</th>
<th>Aspect ratio ( W(\mu m) / L(\mu m) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( M_1, M_3, M_5, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_30 )</td>
<td>2/25</td>
</tr>
<tr>
<td>( M_3, M_6, M_7, M_9, M_{10} )</td>
<td>4/25</td>
</tr>
<tr>
<td>( M_{11}, M_{12}, M_{13}, M_{14} )</td>
<td>16/25</td>
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VI. CONCLUSION
Here using a single DX-MOCCII, two resistors, one capacitor one all-pass filter is designed. Sensitivity with respect to various passive components are found to be very small. The proposed circuit is simulated using PSPICE simulator and 0.25µm technology parameter is used. Theoretical results agree well with the simulated circuit.

REFERENCES