Implementation of Scan Insertion and Compression for 28nm design Technology

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***Abstract* — Scan Insertion and Scan Compression are necessary for design-for-testability (DFT) methodology, which helps to achieve very high quality testability feature for the design at low costs. Scan Insertion methodology is improving over the years and the Scan Compression is improving and meeting the needs by providing the testability feature for the designs. In this paper, the implementation of the Scan Insertion and Compression techniques in the 28nm technology is been presented. We implemented Scan Insertion and compression technology and also, we discuss about the clock and reset DRCs and how the compression help in testing the integrated circuit by reducing the test time and test data volume.**

I. INTRODUCTION

The development in technology scaling will results in increase in power density and heat dissipation due to switching operation of the transistors which results in the damages in the IC, reduction in reliability and less yield. Clock gating, voltage shut-off and other methods must be followed when operated in the functional mode. Preventing heat and power issues during the functional operation conflicts with controllability and observability.DFT technique is proposed to provide the controllability and observability feature for the internal nodes in a design, Controllability means able to change the signal value to the required logic from the inputs and observability means able to observe the changed signal line logic value at the outputs. The paper briefs the implementation of the scan insertion and compression to the design and the way to handle the DRC violations. First focus will be on scan flops conversion in the design and checking for the DRC violations, if there are any DRC violations then fixing them using the commands and after fixing the DRCs scan flops stitching has to be done to form the scan chain and after analysing , it is observed that the number of patterns required will be more due to the more number of scan flops in the single chain. Hence the scan compression is performed in order to reduce the pattern length and tester memory usability. After inserting the scan compression logic again the DRCs has to be verified and if any DRCs found need to be fixed and through scan compression the number of the scan flop stitched in the single chain can decided by compression ratio. This scan insertion and compression is been implemented using the synopsis tool design compiler.

II. RELATED WORK

Heiko Ahrens et al., [1] presented about the implementation and testing of a DFT architecture for a Power PC based microprocessors for various automotive applications which has to result in high quality levels and low test cost. Hence the new architecture consists of dual compression for two different CAD flows but results in overhead of silicon area and engineering resources. So there are two possibilities to overcome this, that is there has to be an agreement between the two companies based on the ATPG and diagnostic tools used, which is very difficult due to financial and technical problems. The second approach is to use the same compression IP by the ATPG and diagnostic tools of the two companies.

A.Chandra et al., [2] proposed industrial view of demonstrating how DFT flows will impact in the presence of compression logic. Hence various DFT architectures are developed using zScan compression technology and discussed pros and cons of each DFT flow with modular DFT insertion. The pin count and scan chain count impact on the QoR(test application time and test data volume requirement). Design teams can use the analysis in this paper to determine DFT strategy for compression. Swapnil Bahl, Shreyans Rungta et al., [3] proposed the different compression schemes DFTMAX. DFTMAX Ultra technology that provides a single solution for all needs. In this paper we discuss the variety of design scenarios from the scan compression point of view. In this paper, they have presented a single compression solution to satisfy the Scan compression requirement for a chip.

Satyendra N. Biswas ,Sunil R. D et al., [4] proposed the way to increase the ATE throughput by vector compression, The compression and decompression algorithm must be simple such that there should not be any pattern loss and should not consume more time to reduce the overall processing time of the ATE. The compression method is based on a hybrid technique which targets on the unique characteristics of the block matching test data compression, BWT along with several coding algorithms reduces the number of transitions for the test vector sequences and results in a high compression ratio in the first stage of the proposed technique.

Prakash Srinivasan, Ronan Farrell et al., [5] Proposed the hierarchical based test architecture in complex SoC designs. However hierarchical test architecture requires additional effort at block level to isolate each block from surrounding blocks and TAM is used to perform scan compression. Based on the analysis the limitations of modular test architecture is known and test plan is for hierarchical architecture is proposed and the test plan feasibility is demonstrated using ATPG tool and thus came to a conclusion that half of the DFT area is reduced by using block isolation.

III. DFT FLOW FOR SCAN INSERTION AND COMPRESSION

First invoke the tool using dc_shell(design compiler) and netlist should be read, the netlist will be in Verilog(.v) or System Verilog(.vs) format using read_file command and set the top module as a current design using the command set current_design. By using the link command, the netlist can be linked with the libraries , the normal flip-flops are converted into scan flip-flop by using the compile -scan command and by defining the configuration type as multiplexed_flip_flop. The clocks ,reset and enable singles are defined using set_dft_signal command, create the scan input and scan output port for all the scan chains using create_port command and define the type of the port (scandatain or scandataout) using -type option in the set_dft_signal command. Define the scan chain path for stitching with the help of set_scan_path command, to create the test default port make use of create_test_protocol command and then check the DRC violations using dft_drc and then fix the respective DRCs and the scan stitching is done.

Then the scan stitching is done using the insert_dft command, the DRC checking is done and DRCs are fixed using the set_auto fix_configuration command and the scan inserted netlist ,reports,.ctl files can be generated using write_test_protocol command.

IV. SCAN COMPRESSION

The scan compression logic reduces the test time and tester memory without loss in the test coverage. The components of the scan compression logic are decompressor and compactor and they are part of scan path, hence functional timing is not affected. Compression logic can be at the design top level or can be placed inside each core of the design. It provides the highest coverage for the design and efficient use of tester pins.

pins, called load-modepins, are dedicated to the MUX select signals.

In the decompressor logic structure every scan cell must be uniquely controllable in every pattern. Only a sparse set of scan cells are required to be controlled in a pattern. As the scan channels increases, in order to provide controllability the number of scan chain increases.

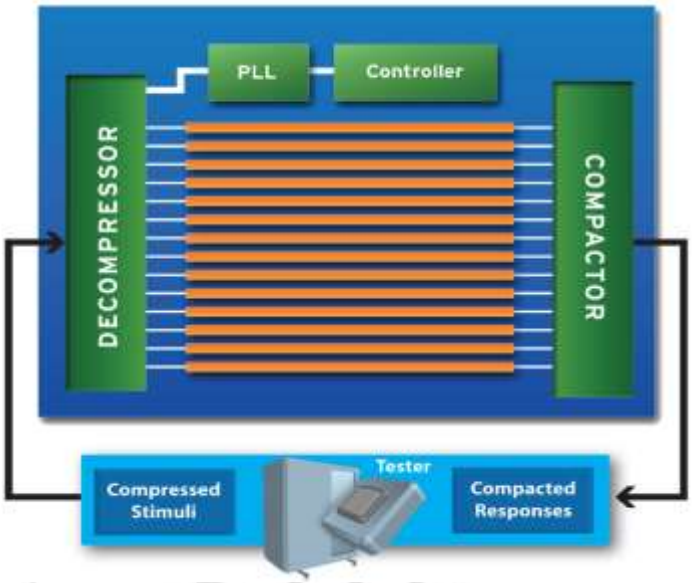

Fig. 1 Scan Compression *The decompressor outputs drives scan-in data pins, either directly or through MUXs. These scan-in data*

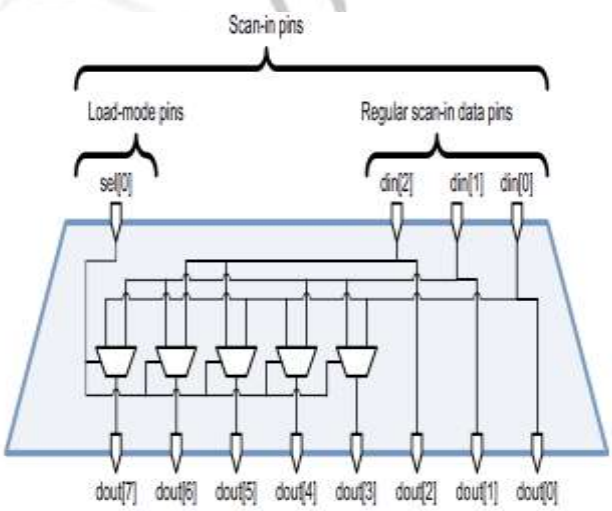

Fig. 2 Decompressor Operation

The compressor outputs drives combinations of compressed scan chains, combined using XOR logic. An fault from a compressed scan chain results in a specific incorrect values at the compressor outputs.
The compressor input are the scan chains. As the compressed scan chain count increases, more XOR configurations are needed. If the chain count is increased, the XOR configurations must repeat, which can impact the diagnosability of the design. As the compressor output channel width increases, the number of fault observed at output port decreases. Thus diagnosability of the design improves, especially when multiple faults diagnosed simultaneously.

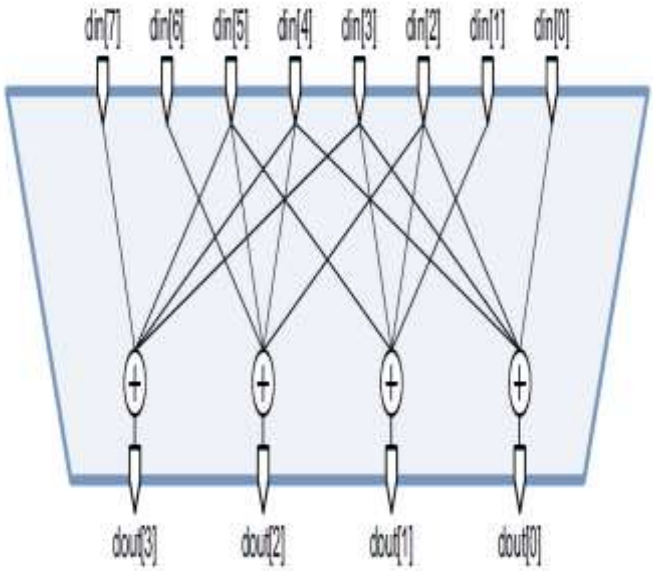

Fig. 3 Compressor Operation

V. RESULTS

Synopsis tool (Design compiler) is used for is used for scan insertion and compression for an 28nm technology. The normal flip-flop conversion into the multiplexed scan flip-flop and scan flip-flop stitching is as shown in the Figure.4 and the chain length depends on the number of scan flip-flops in the design.
The DRC report gives the details about total number of violations occurred after the scan insertion. Hence there are total of 551 violations in which 52 are modeling violations that is 16 cell has unknown model violations and 36 cell has no scan equivalent violations and 464 are LBIST violations and 35 has other violations. Out of 11568 sequential cells 36 cells have violations. The details of the DRC report are as shown in Figure.6.

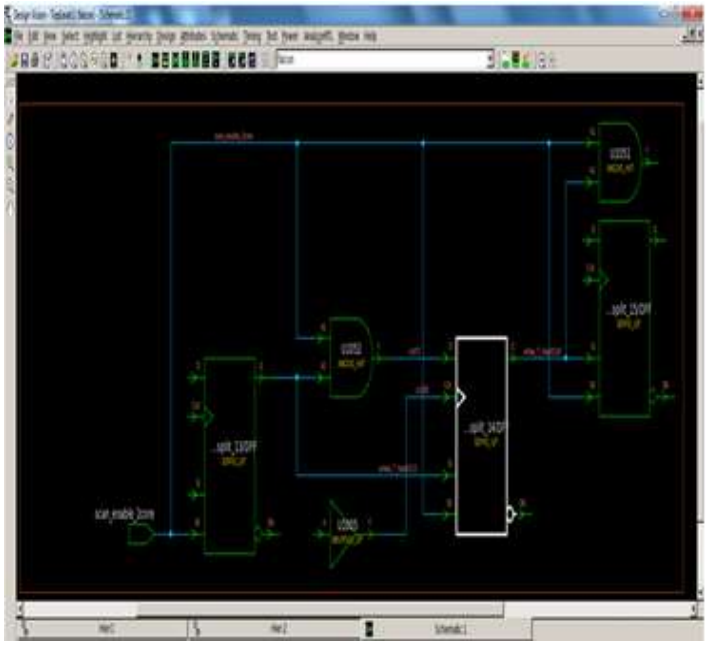

Fig. 4 Scan Stitching

The scan chain information after the scan flow execution is shown in Figure.5

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Number of chains: 10
Scan methodology: full_scan
Scan style: multiplexed_flip_flop
Clock domain: no_mix
Scan enable: scan_enable_2core (no hookup pin)


Scan chain '1' (test_si1 --> BG_scan_out_13) contains 1154 cells


Scan chain '2' (test_si2 --> rwen_2pad[3]) contains 1154 cells


Scan chain '3' (test_si3 --> BG_scan_out_6) contains 1153 cells


Scan chain '4' (test_si4 --> BG_scan_out_4) contains 1153 cells


Scan chain '5' (test_si5 --> test_so5) contains 1153 cells


Scan chain '6' (test_si6 --> BG_scan_out_10) contains 1153 cells


Scan chain '7' (test_si7 --> BG_scan_out_5) contains 1153 cells


Scan chain '8' (test_si8 --> test_so8) contains 1153 cells


Scan chain '9' (test_si9 --> test_so9) contains 1153 cells


Scan chain '10' (test_si10 --> BG_scan_out_11) contains 1153 cells
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Fig. 5 Scan Information

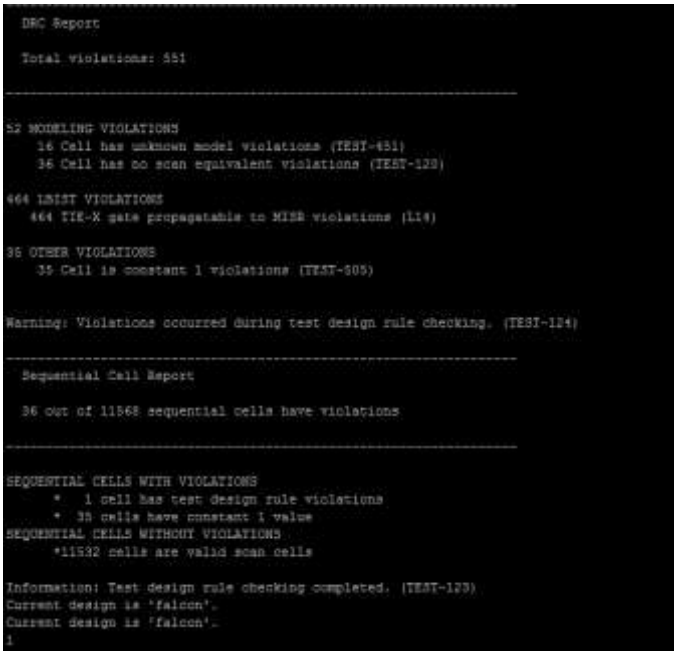

Fig. 6 DRC Report

Two DRC violations observed during scan insertion, one is the clock violation and the other is the reset violation. The clock has to be driven from the port pin, if the clock to a scan flip-flop is driven from any other combinational logic or from data path then the clock violation occurs. Figure.7 shows the clock violation which occurred due to the clock port of the scan flip-flop is driven from the Q output of the other scan flip-flop. Not all flip-flops in the design converts in to the scan flops, for example the flip flops of the shift register in the on chip clock (occ) circuitry.

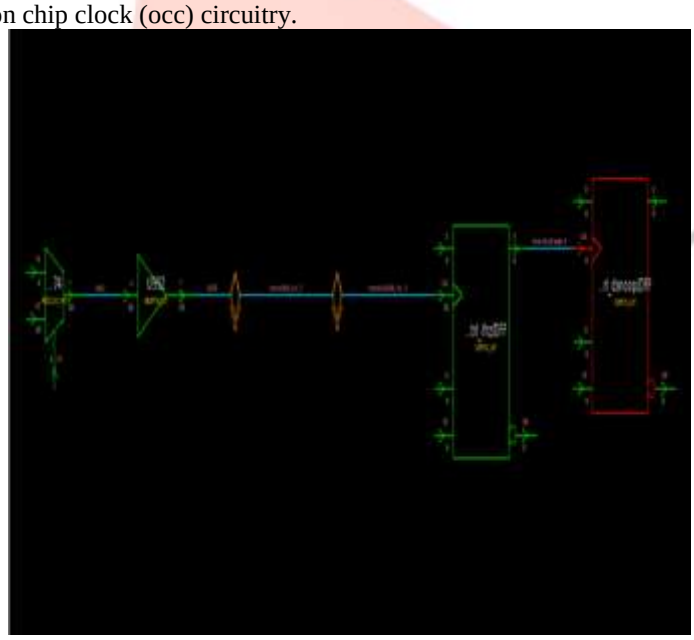

Fig. 7 Clock DRC Violation

Similar to clock pin, the reset pin has to be controlled from the port level, when the reset pin of an flip-flop is not controlled from the port pin then the reset violation occurs. The reset violation observed is an shown in Figure.8.

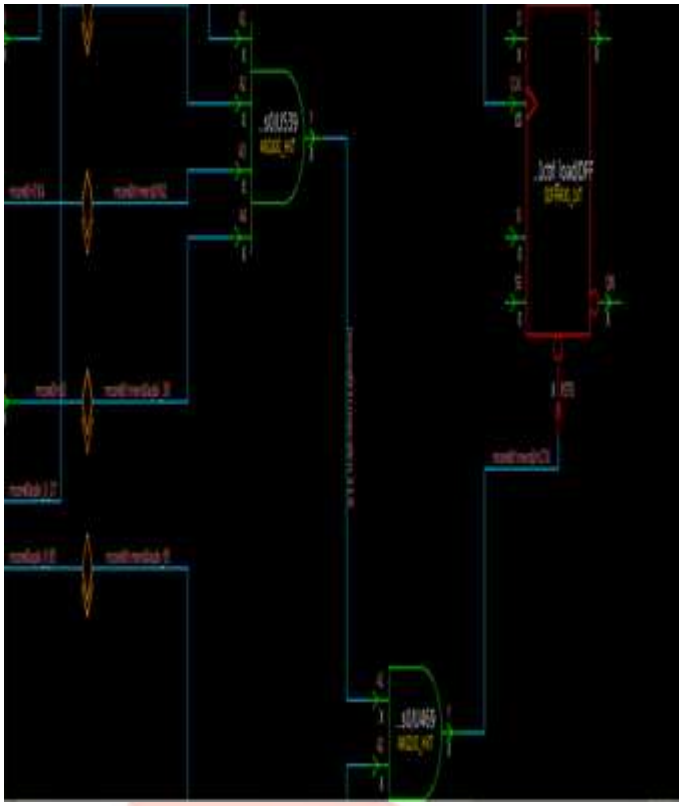

Fig. 8 RESET DRC Violation

In this the reset pin is not controlled from the port level,the reset signal to the flip-flop is coming from the AND gate, hence the controllability of the reset signal is difficult. Thus these DRC s can be fixed using the command set_autofix_configuration command.

For large design without scan compression the pattern length will be more hence more number of shifting cycles required will be more and the tester time and memory will also increase thus in order reduce the tester time and tester memory we introduce scan compression logic in the design.

Scan Compression logic consists of decompressor and comparator logic. The decompressor logic consists of the LFSR(linear shift feedback register) along with the phase shift flip-flops. The decompressor logic distributes the compressed patterns from the input channels to the scan chains. The decompressor logic implemented for the design is as shown in the Figure.9. The number of input channels and scan chains depend on the compression ratio.

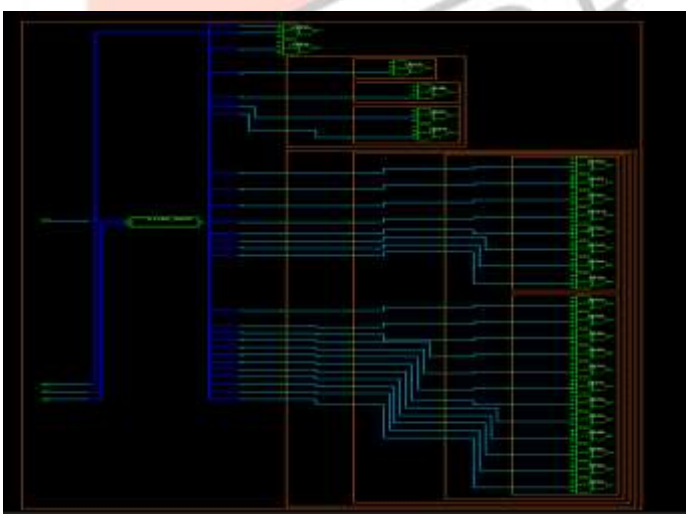

Fig. 9 Decompressor Logic

Compactor logic consists of the EXOR logic, the scan chains are compressed by the EXOR gates in the compactor logic and the output is seen at the output channels. Figure.10 shows the compactor logic.

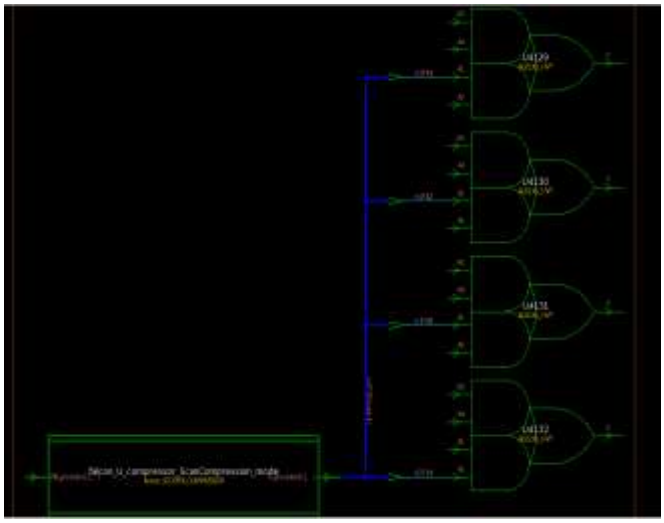

Fig. 10 Compactor Logic

VI. CONCLUSIONS

Aim is to implement the DFT methodology to the 28nm design technology by scan inserting and stitching and by introducing the compressor logic which makes the 28nm design technology testable. Thus, by using the Scan Compression we can reduce the tester time to test the integrated circuit. But as the tool version changes the scan compression logic changes that is new logics are included which simplifies the scan compression. Hence scan insertion and compression DFT steps is implemented on top module which is of 28nm design technology. With better tools the DFT steps can be applied to the further technologies with better coverage. Since the MBIST (Memory Built In Self Test) circuitry consists of flip-flops , so first step in DFT flow is to insert and verify the BIST and boundary scan circuitry and then continue with the scan insertion and compression flow.

VII. REFERENCES

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