# Reduction of Total harmonic distortion in new Cascaded H-Bridge Multilevel Inverter topology using artificial neural network technique

[1]Parveen Nisha.M.G, [2] Pauline Jothi Rajesh. I
[1] PG Student, [2]Assistant Professor
[1]Department of EEE, Info Institute of Engineering, Coimbatore, India

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***Abstract* - This paper deals with reduction of total harmonic distortion in new Cascaded H-bridge multilevel inverter topology with artificial neural network technique. This topology consists of lower blocking voltage on switches and it requires less number of dc voltage sources, power switches which results in decrease the complexity and total cost of the inverter. Moreover, a new algorithm is used to determine the magnitude of dc voltage sources for generation of all voltage levels. Artificial Neural Network (ANN) is trained by the back-propagation algorithm of the Mean Square Error (MSE) between the output and the desired value. The performance and functional accuracy of the proposed topology using ANN technique in generating all voltage levels for 31-level inverter are simulated using MATLAB simulink.**

***Index terms* - Cascaded multilevel inverter, H-bridge, Artificial neural network, Multicarrier pulse width modulation.**

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## I.INTRODUCTION

Nowadays, multilevel inverters have received more attention used for their ability on high-power and medium voltage operation. It has advantages such as high power quality, lower order harmonics, lower switching losses, and better electromagnetic interference. These inverters can generate a stepped voltage waveform by using number of dc voltage sources as input and proper arrangement of the power semiconductor devices. Three main structures of the multilevel inverters are “diode clamped multilevel inverter,” “flying capacitor multilevel inverter,” and “cascaded multilevel inverter”.

The disadvantage of diode clamped multilevel inverter is more complex to control. The main disadvantage of Flying Capacitor Inverter is, the use of more number of capacitors will affect the voltage unbalance across capacitors. To overcome drawbacks like, voltage unbalancing, system shutdown, a topology is developed called Cascaded H – Bridge Inverter. The cascaded multilevel inverter is composed of a number of single-phase H-bridge inverters. It is classified into symmetric and asymmetric group based on the magnitude of dc voltage sources. In the symmetric type, the magnitudes of the dc voltage sources of all H-bridges are equal whereas in the asymmetric type, the values of the dc voltage sources of all H-bridges are different.

In order to increase the number of output voltage levels and to decrease the number of power switches, driver circuits and the total cost of the inverter, a new topology of cascaded multilevel inverters is proposed. In the proposed topology, the unidirectional power switches (IGBT) are used. Finally, the performance of the proposed 31-level inverter through generating all the voltage levels is confirmed by simulation using MATLAB/SIMULINK.

## II.CASCADE MULTILEVEL INVERTER

Cascaded Multilevel Inverter consists of series H-bridge (Full Bridge) Inverter units. Each bridge will be fed from a separate DC source. It consists of sixty unidirectional power switches and forty dc voltage sources. The function of this multilevel inverter is to produce a desired voltage from several Separate Dc Sources (SDCSs). It is more reliable than other two types. Each inverter does not require voltage-clamping diodes or voltage-balancing capacitors unlike in the diode-clamp or flying-capacitors inverter hence inverter bridge produces an output voltage ($+V_{dc}$, 0, $-V_{dc.}$**)**

***Drawbacks:***

- If voltage level increases, the number of switches also increases as a result there is large amount of power loss in the system
- The inverter is very bulky and cost of production is very high.

## III.PROPOSED INVERTER

The proposed Cascade H-Bridge multilevel inverter overcomes the limitation of existing cascade 31-level inverter. In proposed topology, asymmetric type of configuration is used for generating more number of output voltage levels without increase the number of switches and DC voltage sources. It consists of ten unidirectional power switches (IGBT) and four dc

voltage sources. If the power switches of ( $S_{L,1}$, $S_{L,2}$ ) ( $S_{L,3}$, $S_{L,4}$ ) ( $S_{R,1}$, $S_{R,2}$ ) and ( $S_{R,3}$, $S_{R,4}$ ) are turn on simultaneously, the dc voltage sources of ($V_{L,1}$,$V_{L,2}$,$V_{R,1}$,$V_{R,2}$) will be short-circuited, respectively. Hence, the simultaneous turn-on of these switches should be avoided. In addition, $S_a$ and $S_b$ should not turn on simultaneously. The magnitudes of DC voltage sources are must be considered as 1P.U, 5P.U, 2P.U and 10P.U respectively.

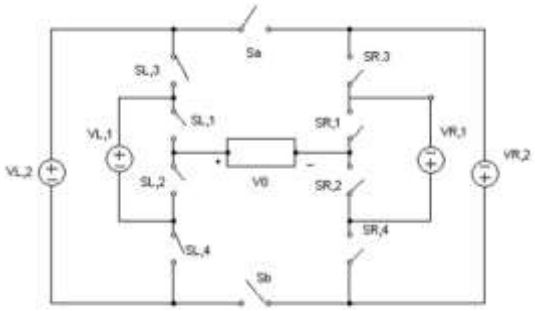


**Figure 1. Circuit Diagram of Proposed Cascaded 31-level Inverter**

***MODES OF OPERATION***

The proposed 31-level inverter circuit is comprise of ten unidirectional switches ($S_a$, $S_b$, $S_{L,1}$, $S_{L,2}$, $S_{L,3}$, $S_{L,4}$, $S_{R,1}$, $S_{R,2}$, $S_{R,3}$, $S_{R,4}$) and four DC voltage sources ($V_{L,1}$, $V_{L,2}$, $V_{R,1}$, $V_{R,2}$ ). The Thirty One Level Cascaded Multilevel Inverter has 31 modes of operation and they are as follows

***(i) Mode 1***

In this mode, the output voltage is ($V_{L,2}$+$V_{R,2}$) to generate this output voltage level, switches $S_{L,1}$, $S_{R,1}$,$S_{L,3}$,$S_{R,3}$ and $S_b$ are turned on. $S_{L,2}$, $S_{R,2}$,$S_{L,4}$,$S_{R,4}$ and $S_a$ are turned off.

***(ii) Mode 2***

In this mode, the output voltage is ($V_{L,2}$+$V_{R,2}$-$V_{L,1}$) to generate this output voltage level, switches $S_{L,1}$, $S_{R,2}$,$S_{L,3}$,$S_{R,3}$ and $S_b$ are turned on. $S_{L,2}$, $S_{R,1}$,$S_{L,4}$,$S_{R,4}$ and $S_a$ are turned off.

***(iii) Mode 3***

In this mode, the output voltage is ($V_{R,2}$+$V_{L,2}$-$V_{R,1}$) to generate this output voltage level, switches $S_{L,2}$, $S_{R,1}$,$S_{L,3}$,$S_{R,3}$ and $S_b$ are turned on. $S_{L,1}$, $S_{R,2}$,$S_{L,4}$,$S_{R,4}$ and $S_a$ are turned off.

***(iv) Mode 4***

In this mode, the output voltage is ($V_{L,2}$+$V_{R,2}$-$V_{L,1}$-$V_{R,1}$) to generate this output voltage level, switches $S_{L,2}$, $S_{R,2}$,$S_{L,3}$,$S_{R,3}$ and $S_b$ are turned on. $S_{L,1}$, $S_{R,1}$,$S_{L,4}$,$S_{R,4}$ and $S_a$ are turned off.

***(v) Mode 5***

In this mode, the output voltage is ($V_{L,1}$+$V_{R,2}$) to generate this output voltage level, switches $S_{L,1}$, $S_{R,1}$,$S_{L,3}$,$S_{R,4}$ and $S_b$ are turned on. $S_{L,2}$, $S_{R,2}$,$S_{L,4}$,$S_{R,3}$ and $S_a$ are turned off.

***(vi) Mode 6***

In this mode, the output voltage is ($V_{R,2}$) to generate this output voltage level, switches $S_{L,1}$, $S_{R,2}$,$S_{L,3}$,$S_{R,4}$ and $S_b$ are turned on. $S_{L,2}$, $S_{R,1}$,$S_{L,4}$,$S_{R,3}$ and $S_a$ are turned off.

***(vii) Mode 7***

In this mode, the output voltage is ($V_{L,1}$-$V_{R,1}$+$V_{R,2}$) to generate this output voltage level, switches $S_{L,1}$, $S_{R,1}$,$S_{L,3}$,$S_{R,4}$ and $S_b$ are turned on. $S_{L,2}$, $S_{R,2}$,$S_{L,4}$,$S_{R,3}$ and $S_a$ are turned off.

***(viii) Mode 8***

In this mode, the output voltage is ($V_{R,2}$-$V_{R,1}$) to generate this output voltage level, switches $S_{L,1}$, $S_{R,2}$,$S_{L,3}$,$S_{R,4}$ and $S_b$ are turned on. $S_{L,2}$, $S_{R,1}$,$S_{L,4}$,$S_{R,3}$ and $S_a$ are turned off.

***(ix) Mode 9***

In this mode, to generate output voltage level ($V_{L,2}$+$V_{R,1}$), switches $S_{L,1}$, $S_{R,1}$,$S_{L,4}$,$S_{R,3}$ and $S_b$ are turned on. $S_{L,2}$, $S_{R,2}$,$S_{L,3}$,$S_{R,4}$ and $S_a$ are turned off.

***(x) Mode 10***

In this mode, to generate output voltage level ($V_{L,2}+V_{R,1}-V_{L,1}$), switches $S_{L,1}$, $S_{R,2}$,$S_{L,4}$,$S_{R,3}$ and $S_b$ are turned on. $S_{L,2}$, $S_{R,1}$,$S_{L,3}$,$S_{R,4}$ and $S_a$ are turned off.

***(xi) Mode 11***

In this mode, the output voltage ($V_{L,2}$) to generate this output voltage level, switches $S_{L,2}$, $S_{R,1}$,$S_{L,4}$,$S_{R,3}$ and $S_b$ are turned on. $S_{L,1}$, $S_{R,2}$,$S_{L,3}$,$S_{R,4}$ and $S_a$ are turned off.

***(xii) Mode 12***

In this mode, the output voltage is ($V_{L,2}-V_{L,1}$) to generate this output voltage level, switches $S_{L,2}$, $S_{R,2}$,$S_{L,4}$,$S_{R,3}$ and $S_b$ are turned on. $S_{L,1}$, $S_{R,1}$,$S_{L,3}$,$S_{R,4}$ and $S_a$ are turned off.

***(xiii) Mode 13***

In this mode, the output voltage is ($V_{L,1}+V_{R,1}$) to generate this output voltage level, switches $S_{L,1}$, $S_{R,1}$,$S_{L,4}$,$S_{R,4}$ and $S_b$ are turned on. $S_{L,2}$, $S_{R,2}$,$S_{L,3}$,$S_{R,3}$ and $S_a$ are turned off.

***(xiv) Mode 14***

In this mode, the output voltage is ($V_{R,1}$) to generate this output voltage level, switches $S_{L,1}$, $S_{R,2}$,$S_{L,4}$,$S_{R,4}$ and $S_b$ are turned on. $S_{L,2}$, $S_{R,1}$,$S_{L,3}$,$S_{R,3}$ and $S_a$ are turned off.

***xv) Mode 15***

In this mode, the output voltage is ($V_{L,1}$), to generate this output voltage level, switches $S_{L,2}$, $S_{R,1}$,$S_{L,4}$,$S_{R,4}$ and $S_b$ are turned on. $S_{L,1}$, $S_{R,2}$,$S_{L,3}$,$S_{R,3}$ and $S_a$ are turned off.

***(xvi) Mode 16***

In this mode, the output voltage is Zero to generate this output voltage level, switches $S_{L,1}$, $S_{R,1}$,$S_{L,3}$,$S_{R,3}$ and $S_a$ are turned on. $S_{L,2}$, $S_{R,2}$,$S_{L,4}$,$S_{R,4}$ and $S_b$ are turned off or vice versa.

***(xvii) Mode 17***

In this mode, the output voltage is ($-V_{L,1}$) to generate this output voltage level, switches $S_{L,1}$, $S_{R,2}$,$S_{L,3}$,$S_{R,3}$ and $S_a$ are turned on. $S_{L,2}$, $S_{R,1}$,$S_{L,4}$,$S_{R,4}$ and $S_b$ are turned off.

***(xviii) Mode 18***

In this mode, to generate output voltage level ($-V_{R,1}$), switches $S_{L,2}$, $S_{R,1}$,$S_{L,3}$,$S_{R,3}$ and $S_a$ are turned on. $S_{L,1}$, $S_{R,2}$,$S_{L,4}$,$S_{R,4}$ and $S_b$ are turned off.

***(xix) Mode 19***

In this mode, -( $V_{L,1}+ V_{R,1}$) to generate this output voltage level, switches $S_{L,2}$, $S_{R,2}$,$S_{L,3}$,$S_{R,3}$ and $S_a$ are turned on. $S_{L,1}$, $S_{R,1}$,$S_{L,4}$,$S_{R,4}$ and $S_b$ are turned off.

***(xx) Mode 20***

In this mode, the output voltage is $-(V_{L,2}-V_{L,1})$, to generate this output voltage level , switches $S_{L,1}$, $S_{R,1}$,$S_{L,3}$,$S_{R,4}$ and $S_a$ are turned on. $S_{L,2}$, $S_{R,2}$,$S_{L,4}$,$S_{R,3}$ and $S_b$ are turned off.

***(xxi) Mode 21***

In this mode, to generate the output voltage level ($-V_{L,2}$), switches $S_{L,1}$, $S_{R,3}$,$S_{L,3}$,$S_{R,4}$ and $S_a$ are turned on. $S_{L,2}$, $S_{R,2}$,$S_{L,4}$,$S_{R,2}$ and $S_b$ are turned off.

***(xxii) Mode 22***

In this mode, the output voltage is $-(V_{L,2}+V_{R,1}-V_{L,1})$ to generate this output voltage level, switches $S_{L,2}$, $S_{R,1}$,$S_{L,3}$,$S_{R,4}$ and $S_a$ are turned on. $S_{L,1}$, $S_{R,2}$,$S_{L,4}$,$S_{R,3}$ and $S_b$ are turned off.

***(xxiii) Mode 23***

In this mode, the output voltage is -( $V_{L,2}+ V_{R,1}$) to generate this output voltage level, switches $S_{L,2}$, $S_{R,2}$,$S_{L,3}$,$S_{R,4}$ and $S_a$ are turned on. $S_{L,1}$, $S_{R,1}$,$S_{L,4}$,$S_{R,3}$ and $S_b$ are turned off.

***(xxiv) Mode 24***

In this mode, the output voltage is $-(V_{R,2}-V_{R,1})$ to generate this output voltage level, switches $S_{L,1}$, $S_{R,1}$,$S_{L,4}$,$S_{R,3}$ and $S_a$ are turned on. $S_{L,2}$, $S_{R,2}$,$S_{L,3}$,$S_{R,4}$ and $S_b$ are turned off.

***(xxv) Mode 25***

In this mode, the output voltage is -( $V_{L,1}- V_{R,1}+V_{R,2}$) to generate this output voltage level, switches $S_{L,1}$, $S_{R,2}$,$S_{L,4}$,$S_{R,3}$ and $S_a$ are turned on. $S_{L,2}$, $S_{R,1}$,$S_{L,3}$,$S_{R,4}$ and $S_b$ are turned off.

***(xxvi) Mode 26***

In this mode, the output voltage is ($-V_{R,2}$) to generate this output voltage level, switches $S_{L,2}$, $S_{R,1}$,$S_{L,4}$,$S_{R,3}$ and $S_a$ are turned on. $S_{L,1}$, $S_{R,2}$,$S_{L,3}$,$S_{R,4}$ and $S_b$ are turned off.

***(xxvii) Mode 27***

In this mode, to generate the output voltage level $-(V_{L,1}+V_{R,2})$, switches $S_{L,2}$, $S_{R,2}$,$S_{L,4}$,$S_{R,3}$ and $S_a$ are turned on. $S_{L,1}$, $S_{R,1}$,$S_{L,3}$,$S_{R,4}$ and $S_b$ are turned off.

***(xxviii) Mode 28***

In this mode, to generate output voltage $[-(V_{L,2}+V_{R,2}-V_{L,1}-V_{R,1})]$,switches $S_{L,1}$, $S_{R,1}$,$S_{L,4}$,$S_{R,4}$ & $S_a$ are turned on.$S_{L,2}$, $S_{R,2}$,$S_{L,3}$,$S_{R,3}$& $S_b$ are turned off.

***(xxix) Mode 29***

In this mode, the output voltage is $[-(V_{R,2+}V_{L,2}-V_{R,1})]$ to generate this output voltage level, switches $S_{L,1}$, $S_{R,2}$,$S_{L,4}$,$S_{R,4}$ and $S_a$ are turned on. $S_{L,2}$, $S_{R,1}$,$S_{L,3}$,$S_{R,3}$ and $S_b$ are turned off.

***(xxx) Mode 30***

In this mode, the output voltage is $-(V_{L,2}+V_{R,2}-V_{L,1})$ to generate this output voltage level, switches $S_{L,2}$, $S_{R,1}$,$S_{L,4}$,$S_{R,4}$ and $S_a$ are turned on. $S_{L,1}$, $S_{R,2}$,$S_{L,3}$,$S_{R,3}$ and $S_b$ are turned off.

***(xxxi) Mode 31***

In this mode, the output voltage is $-(V_{L,2}+V_{R,2})$ to generate this output voltage level, switches $S_{L,2}$, $S_{R,2}$,$S_{L,4}$,$S_{R,4}$ and $S_a$ are turned on. $S_{L,1}$, $S_{R,1}$,$S_{L,3}$,$S_{R,3}$ and $S_b$ are turned off.

## IV.MULTICARRIER PULSE WIDTH MODULATION

In this paper, Multicarrier Pulse Width Modulation is used to control the output voltage and reduce the harmonics. For an n-level inverter, n-1 carriers with the same frequency and the same amplitude are disposed such that the bands they occupy are contiguous. The reference waveform has maximum amplitude and frequency and it is zero centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals to obtain the necessary gating pulses. If the reference is greater than a carrier signal, then the IGBT corresponding to that carrier be switched on and if the reference is less than a carrier signal, then the IGBT corresponding to that carrier be switched off. The phases of carrier signals are rearranged to produce three main disposition techniques known as PD, POD and APOD.

***Phase Disposition Modulation Method (PDPWM)***

In phase disposition method all the carriers have the same frequency, amplitude and are in phase. It is based on a comparison of a sinusoidal reference waveform with vertically shifted carrier waveform as shown in figure 3. This method uses N –1 carrier signals to generate N level inverter output voltage. In this method fourteen triangular carrier wave have compared with the one sinusoidal reference wave.

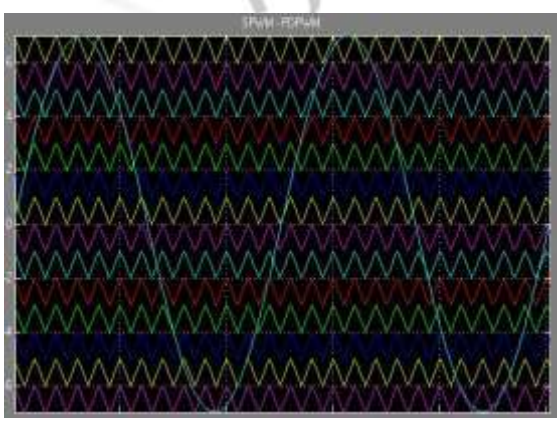

**Figure 2. Phase Disposition Modulation**

## V. ARTIFICIAL NEURAL NETWORK TECHNIQUE

An artificial neural network is mathematical or computational models that try to simulate the structure and functional aspects of biological neural networks. In most cases, ANN is an adaptive system that changes structure based on external or internal information which flows throughout the network during the learning phase. Neural networks are non-linear statistical data modeling tools. They can be used as model complex relationships between inputs and outputs or to find data patterns. The Artificial neural network is trained by the back-propagation algorithm of the Mean Square Error (MSE) between the output and the desired value. The training set for the network has been produced off-line by solving these non-linear equations using Newton-Raphson method.

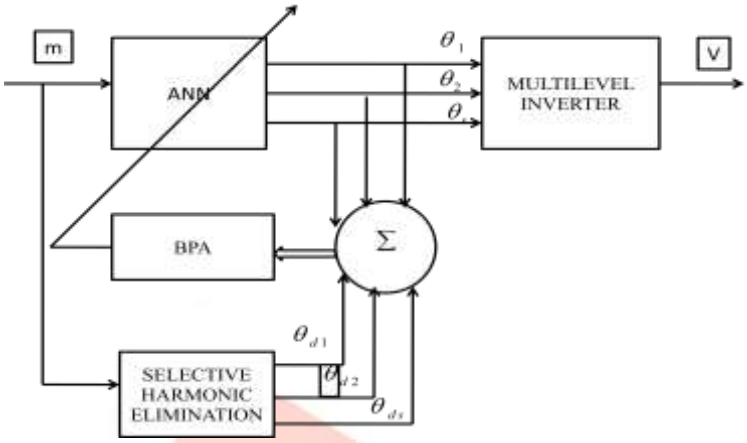


**Figure 3. Back Propagation Algorithm**

To implement this algorithm, MATLAB programming is used which in turn makes the process fast and easy. When a set of input values are presented in the ANN, step by step calculations are made in forward direction to drive the output pattern. The mean square error (MSE) generated for the set of input patterns, it is minimized by gradient descent method altering the weights one at a time starting from the output layer. After the termination of training phase, the obtained ANN is used to generate the control sequence of the inverter. ANN is also used for the generation of the optimal switching angles, which has a single input neuron fed by the modulation index, one hidden layer and s outputs where each output represents a switching angle. This set of angles is required to eliminate the 5th, 7th, 11th and 13th harmonics, etc,

## VI. SIMULATION RESULTS

Cascaded H-Bridge Multilevel Inverter Topology with Artificial Neural Network Technique designed and simulated using the MATLAB/SIMULINK Software. Based on DC source algorithm, if the magnitude of ($V_{L,1}$) considered as 15 V, then the magnitudes of other dc voltage sources will be 30, 75, and 150 V, which are related to ($V_{R1}$, $V_{L2}$, and $V_{R2}$) respectively. Now, the magnitude of ($V_{R1}$) DC source is changed as 40V and the THD will be 5.64%. Fig: 9 shows the voltage of ANN is 225V and current of are 22.5 Ampere waveform of Cascade H-Bridge 31-Level inverter. Fig: 8 show the simulink model of artificial neural network technique for cascaded H-Bridge multilevel inverter. Table (1) shows the system parameters used for simulation. Table (2) shows the switching patterns and output voltages of each level of Cascaded H-Bridge 31-level Inverter.

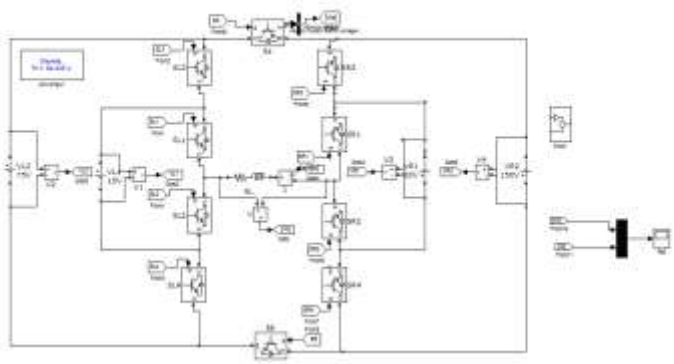

**Figure 4. Simulink Model of Artificial Neural Network Technique for Cascaded H-Bridge 31-Level Inverter**

**Table 1. Parameters and Values of Cascaded H-Bridge 31-Level Inverter**

| S.NO | Parameters | Values of simulation |
|---|---|---|
| 1 | DC supply voltage ($V_{dc}$) | 270V |
| 2 | Inductance (L) | $49 \times 10^{-3}$ H |
| 3 | Switching frequency | 50 HZ |
| 4 | Snubber Resistance ($R_s$) | 148Ω |
| 5 | Diode Resistance ($R_d$) | 0.05Ω |
| 6 | Output voltage | 225V |
| 7 | Load Resistance | 10 Ω |

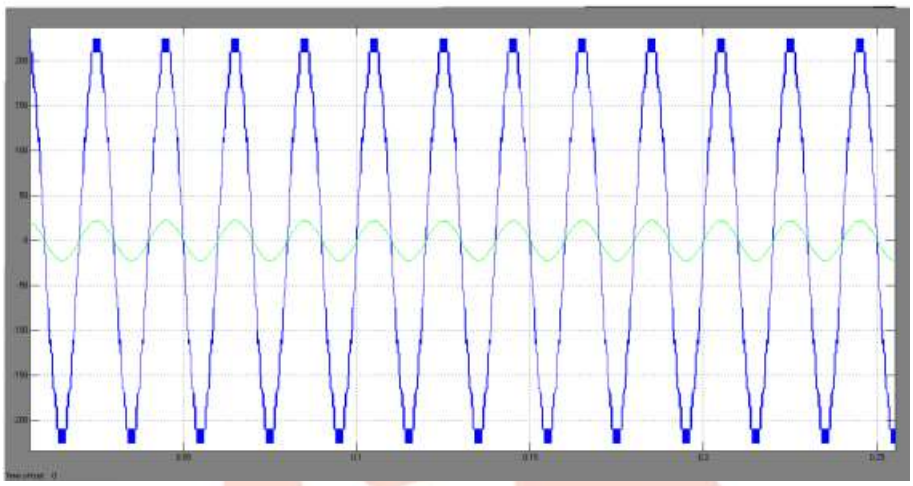

**Figure 5. Output Voltages and Current of Inverter**

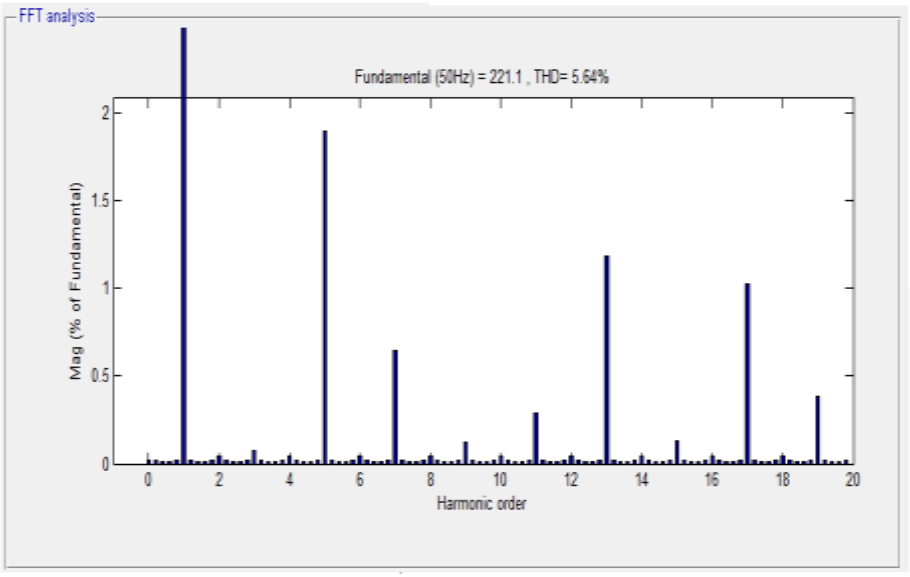


**Figure 6. THD Analysis of Inverter**

**Table 3. Comparison of THD Analysis**

| S.NO | Magnitude of DC source | THD of existing cascade H-Bridge 31-level Inverter | THD of proposed cascade H-Bridge 31-level Inverter |
|---|---|---|---|
| 1 | $V_{L,1}$=15V ,$V_{L,2}$=65 V,$V_{R,1}$=30V $V_{R,2}$=150V | 5.11% | 4.72% |
| 2 | $V_{L,1}$=15V ,$V_{L,2}$=65V,$V_{R,1}$=40V $V_{R,2}$=150V | 6.14% | 5.56% |
| 3 | $V_{L,1}$=15V ,$V_{L,2}$=75V,$V_{R,1}$=40V $V_{R,2}$=150V | 5.81% | 5.64% |
| 4 | $V_{L,1}$=15V ,$V_{L,2}$=75V,$V_{R,1}$=40V $V_{R,2}$=160V | 5.12% | 5.01% |
| 5 | $V_{L,1}$=15V ,$V_{L,2}$=65V,$V_{R,1}$=30V $V_{R,2}$=160V | 5.84% | 5.39% |
| 6 | $V_{L,1}$=15V ,$V_{L,2}$=65V,$V_{R,1}$=50V $V_{R,2}$=170V | 7.88% | 7.56% |
| 7 | $V_{L,1}$=15V ,$V_{L,2}$=65V,$V_{R,1}$=50V $V_{R,2}$=150V | 9.27% | 8.64% |

Table (3) represents the THD analysis of existing and proposed cascaded H-bridge 31-level inverter with different combination of change in magnitude of DC voltage source.

**Table 2. Switching Patterns and Output Voltages of the 31-level Inverter**

| NO | $S_{L,1}$ | $S_{L,2}$ | $S_{L,3}$ | $S_{L,4}$ | $S_{R,1}$ | $S_{R,2}$ | $S_{R,3}$ | $S_{R,4}$ | $S_a$ | $S_b$ | $V_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | $V_{L,2}+V_{R,2}$ |
| 2 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | $V_{L,2}+V_{R,2}-V_{L,1}$ |
| 3 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | $V_{R,2}+V_{L,2}-V_{R,1}$ |
| 4 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | $(V_{L,2}+V_{R,2}-V_{L,1}-V_{R,1})$ |
| 5 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | $V_{L,1}+V_{R,2}$ |
| 6 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | $V_{R,2}$ |
| 7 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | $V_{L,1}-V_{R,1}+V_{R,2}$ |
| 8 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | $V_{R,2}-V_{R,1}$ |
| 9 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | $V_{L,2}+V_{R,1}$ |
| 10 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | $V_{L,2}+V_{R,1}-V_{L,1}$ |
| 11 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | $V_{L,2}$ |
| 12 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | $V_{L,2}-V_{L,1}$ |
| 13 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | $V_{L,1}+V_{R,1}$ |
| 14 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | $V_{R,1}$ |
| 15 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | $V_{L,1}$ |
| 16 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | |
| 17 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | $-V_{L,1}$ |
| 18 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | $-V_{R,1}$ |
| 19 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | $-(V_{L,1}+V_{R,1})$ |
| 20 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | $-(V_{L,2}-V_{L,1})$ |
| 21 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | $-V_{L,2}$ |
| 22 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | $-(V_{L,2}+V_{R,1}-V_{L,1})$ |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 23 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | -( $V_{L,2}$+ $V_{R,1}$) |
| 24 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | -($V_{R,2}$-$V_{R,1}$) |
| 25 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | -( $V_{L,1}$- $V_{R,1}$+$V_{R,2}$) |
| 26 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | -$V_{R,2}$ |
| 27 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | -($V_{L,1}$+$V_{R,2}$) |
| 28 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | -($V_{L,2}$+$V_{R,2}$- $V_{L,1}$-$V_{R,1}$) |
| 29 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | -($V_{R,2+}V_{L,2}$- $V_{R,1}$) |
| 30 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | -($V_{L,2}$+$V_{R,2}$- $V_{L,1}$) |
| 31 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | -($V_{L,2}$+$V_{R,2}$) |

## VII. CONCLUSION

This paper deals with the Cascaded H-Bridge Multilevel Inverter with artificial neural network technique. The proposed general topology was compared with the different kinds of presented topologies from different points of view. According to the comparison results, the proposed topology requires a lesser number of IGBTs, power diodes, driver circuits, and dc voltage sources. Multicarrier Pulse Width Modulation method is used to control Cascaded H-Bridge Multilevel Inverter. In this paper, artificial neural network technique is used to control the output voltage and to reduce harmonics of Cascaded H-Bridge Multilevel Inverter. If the magnitude of dc sources increases or decreases, it will affect the output voltage and also increases the THD value. Using ANN technique, the THD value of inverter can be reduced. The THD value is 5.64% and output voltage is 225V. The performance accuracy of the Cascaded H-Bridge 31-level inverter was verified through the MATLAB/SIMULINK.

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