Layout Designing and Transient Analysis of Carry Lookahead Adder Using 300nm Technology-A Review

Lily Kanoriya, Aparna Gupta, Dr. Soni Changlani
M.Tech Student, Assistant Professor, Head of Department
Department of Electronics and Communication Engineering, Rajiv Gandhi Proudyogiki Vishwavidyalaya
Lakshmi Narain College of Technology & Science,Bhopal, India

***Abstract*— Adders are not only used for addition but it is also important in multiplication, division, and in address calculation. Carry Look Ahead Adder is very efficient adder since it can save the time of propagating the carry bits. This paper discusses the review of design of an Integrated Circuit(IC) layout for different bits of Carry Look Ahead Adder using full custom method with 300nm scaling.The layout will be design by using an open source software namely electric VLSI design system. In order to produce the layout, the basic knowledge of fabrication process and IC design rule is necessary. The layout will go for Design Rule Check set by the electric VLSI design system to check for any design rule error. Both layout and schematic circuit of CLA were then going to simulate through Layout versus Schematic to ensure they both are identical. LT Spice IV will be used as a simulator to carry out the simulation work and verifying the validity of the circuit function. Through the correspondence of the layout design we can go for the analysis of transient and frequency response of CLA.**

***Index Terms* - Carry Look Ahead Adder (CLA), Schematic, IC Layout, Electric VLSI design system , LT Spice IV.**

I. INTRODUCTION

Many electronic devices have been widely used in different fields and the size of these devices has been gradually decreased day by day. This is only possible because of contribution of different IC technologies. An example in today's era is the mobile phone which is made smaller to enhance user's mobility and usage time. With this technology, the modern devices have been reduced to convenient sizes. Besides that, mass production of IC has lowered the cost and made most electronic devices affordable. Today, an IC is very small or tiny size and can hold millions of transistors. Hence, further research in the design of IC is very important to enhance the production of a more efficient and reliable IC.

There are different technologies used to construct integrated circuit such as NMOS technology, PMOS technology, bipolar technology and CMOS technology. In this paper, we will use CMOS technology because it consumes less power as power is used only when NMOS and PMOS transistors are switching between on & off states.

Rest of paper discusses about CLA in section (ii), About IC design in section (iii), CLA layout review in section (iv), methodology in section (v) & in last conclusion of this paper.

II. CLA ADDER OVERVIEW.

Addition is the very basic operation in the digital electronics. But most of the digital component takes time to propagate the carry signal. With the use of Carry Look Ahead Adder, we can reduce the time required for the carry bits.

Next we discussed the basic structure of CLA. CLA uses two signals P & G (PROPAGATE SIGNAL & GENERATE SIGNAL).

Table 1 – Truth Table

A_i	B_i	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1 shows the truth table of binary addition. When A_i, B_i and C_{in} are high, then the sum will be high and carry will also be generated.

The expression for the carry propagate Pi as shown in equation (1), generate signal G_i in equation (2), sum in equation (3), and carry out C_{i+1} in equation (4).

$$\boldsymbol{P_i = A_i \oplus B_i} \quad \textbf{(1)}$$

$$\boldsymbol{G_i = A_i . B_i} \quad \textbf{(2)}$$

The output sum and carry can be expressed as

$$\boldsymbol{S_i = P_i \oplus C_i} \quad \textbf{(3)}$$

$$\boldsymbol{C_{i+1} = G_i + (P_i . C_i)} \quad \textbf{(4)}$$

Where i = 0,1,2…..n-1**.**

For 4 bit CLA-

Having the above equation we could design the circuit. We can now write the Boolean function for the carry output of each n (here 4) stage and substitute for each Ci.

Apply previous equations for a 4 bit CLA. The output carry equations are given below:

$C_1 = G_0 + P_0C_0$

$C_2 = G_1 + P_1C_1 = G_1 + P_1(G_0 + P_0C_0) = G_1 + P_1G_0 + P_1P_0C_0$

$C_3 = G_2 + P_2C_2 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0$

$C_4 = G_3 + P_3C_3 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1 P_0C_0$.

The equations of propagate, generate, sum and carry signal are going to repeat for n number of bits such as for 8, 16, 32 etc.

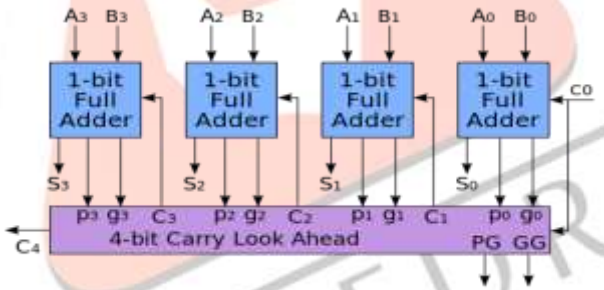

Figure 1 - 4 bit CLA using full adder.

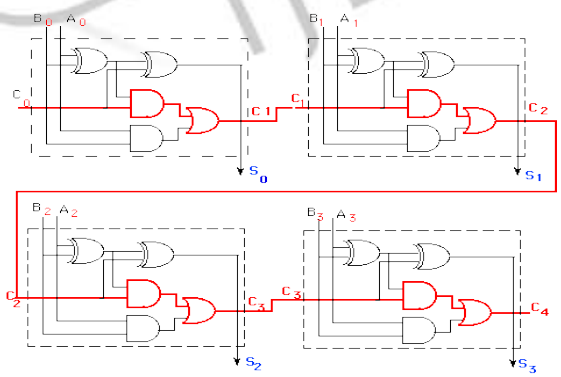

Figure 2 – 4 bit CLA adder using logic gates.

Fig.1 shows the CLA adder using 1 bit full adder[5]. The output of the full adder is carry propagate, carry generate and the sum of respective bits. The carry propagate and carry generate bits are given to the carry look ahead adder and the final carry is generated by CLA generator. Fig.2 shows the carry look ahead adder using logic gates such as Exclusive OR gate, AND gate, and OR gate.

III. IC DESIGN

IC layout are built from three components, basically used components are transistor, wires and vias. During the design of layouts, design rules have to be followed. A design rule governs the layout of individual component and interaction between those components. When designing an IC, designers tend to make the components as small as possible & enabling implementation of as many functions onto a single chip. Since these wires and transistor are so small, errors may occur during the fabrication process. Hence to minimize the errors during fabrication process design rules created. Formulation of design rule helps to increase the yield of correct chip to a suitable level. Therefore, it is important to consider the design rule during layout designing.

The verification process which will be used in this project involves DRC (Design Rule Check), LVS (Layout Versus Schematic) & ERC (Electrical Rule Check). These are important procedures in IC layout and they cannot be considered roughly.

A) DRC(Design Rule Check)

DRC is a verification process that determines whether the physical layout of the chip satisfies the design rules or not. It ensures that all the layers meet manufacturing process such as the width and space rule. DRC is the first level of verification once the layout is ready. DRC not only checks the design rules but also it goes through the design placed within the context in which it is going to be used. The possibility of errors in the design will be reduced and a high reliability of design will be achieved. Therefore it provides an instant analysis, but not the complete one.

B) LVS(Layout Versus Schematic)

LVS is a process to check whether a particular IC layout corresponds to the original schematic circuit of the design or not. The schematic acts as the reference circuit and the layout will be checked against it. In this process, electrical connectivity of all signals, including the input, output and power signals to their corresponding devices are checked. Besides that, the sizes of the device will also be checked including the width and length of transistor, sizes of resistors and capacitors The LVS also identify the extra components and the signals that have not been included in the schematic. In Electric VLSI Design system, this type of checking is known as the Networking Consistency Check. NCC firsts attempts is to discover the circuit mismatches using a algorithm called local partitioning. After that NCC uses Gemini algorithm, a second generation layout validation program.

C) ERC(Electrical Rule Check)

ERC is usually used to check the errors in connectivity or connection of devices .It is an optional choice of checking.ERC is used to check for any unconnected, partly connected or redundant devices Also check for any disabled transistors, floating nodes and short circuits.

Table 2 – Design Rules.

LAYER	WIDTH	SPACE
Poly	2	3
Diff	3	3
Metal 1	3	3
Metal 2	3	4
N well	12	6
Cut	2	2
Via	2	3

Table -2 shows the fundamental rule of designing an IC, all values are in lambda[9]. It shows the design rule of diffusion, poly, metal 1, metal 2, cut, via. Alignment rule for cut or via surround and poly space to diffusion is 1λ. And for poly overlap diffusion is 2λ.

IV. CLA LAYOUT REVIEW.

In VLSI System, layout designing of CLA has been performed using various technologies.

In this paper[1], the author has given a method of designing an IC layout using 90nm technology. In which both semi-custom and fully custom method was used. And the performance of CLA was measured by comparing the result of semi custom and full custom in terms of power dissipation and area efficiency. The result shows that, semi custom method gives slow power consumption and small area in comparison with fully custom method.

This paper[2], aims on a concept of Short Pulse Power Gated Approach (SPOGA), a leakage power reduction technique. The analysis of the circuit was done by using 90nm technology in cadence GPDK. The values of power consumption of the circuit are interpreted from the transient analysis. The result shows that, the short pulse activated the logic block only for the needed short duration thereby reduced the unnecessary consumption.

In this paper[3], CD(Constant Delay) logic was used for reducing the power dissipation and for the power delay product. Simulation was done by using H-Spice and delay was checked by Cosmo Scope Z 2007.03 software. The CD logic primarily concentrate on delay improvement at the critical path and yields better PDP.

In this paper[4], different static and dynamic logic styles (such as CMOS,DCVS Pseudo NMOS,PTL &Domino logic) was used for the implementation of CLA. The performance was measured by comparing the result in terms of propagation delay, power dissipation, and their delay product. Simulation of circuit was done with the Tanner EDA tool, and considering different features size 150nm, 200nm, and 250nm.The result of this paper gives that minimum average power required in case of 4 bit standard CMOS CLA, and maximum average power for the 8 bit pseudo NMOS CLA implementation.

This paper[5], focuses on the implementation and simulation of 4 bit, 8 bit & 16 bit of CLA based on verilog code and compared their performance in terms of area, delay, area delay product by using Xilinx as synthesis tool. The result show that carry look ahead adder had least area delay product.

In this paper[6], different type of 8 bit adders are analyzed and compared for transistor count power dissipation, delay and power delay product. The performance was measured by comparing the result in terms of power dissipation and PDP. Simulation was done using Tanner environment with 90nm and 180nm technology. The result shows that the carry skip adder and carry look ahead adder uses least number of transistors. And carry skip adder has least PDP (Power Delay Product.).

In this paper[7], the author has given an alternative log n stage design which is nearly optimum with respect to regularity, area time efficiency ,and maximum interconnection wire length. The layout of CLA is highly regular when input output restriction, the addition of two n-bit numbers can be performed in time 0(log n).

V. METHODOLOGY

We are going to deal with Electric Cad software. And exploit its powerful tools. And will use LT Spice IV simulation software for the schematic capture and wave viewer. CLA consists of XOR, AND, & OR gates. Through gates we can design carry generate and propagate signal. Fig 3 shows the schematic diagram of propagate and generate signal. It is going to use in every stage of CLA either it is of 4, 8, 16, 32 bit or many more. Fig 4 shows the schematic diagram of 1 bit partial full adder and fig 6 shows the schematic diagram of 4 bit CLA.

In every stage of layout designing, we will do DRC check, to identify any error. After designing of layout we will do the LVS check. If both DRC and LVS were identical, then we will go for transient analysis and frequency response of CLA.

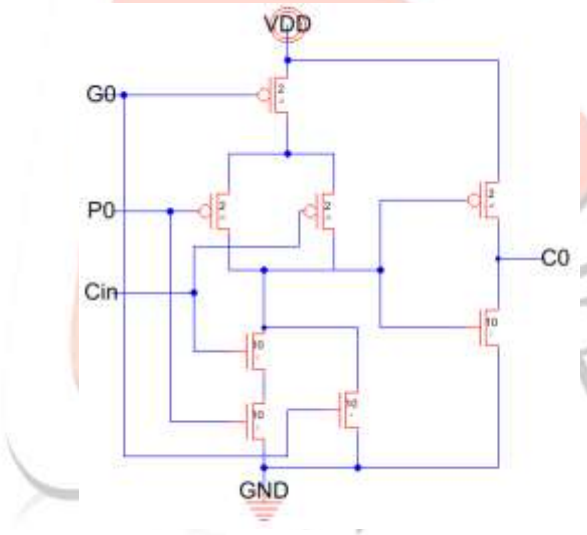

Figure 3 – Schematic of propagates and generate signal.

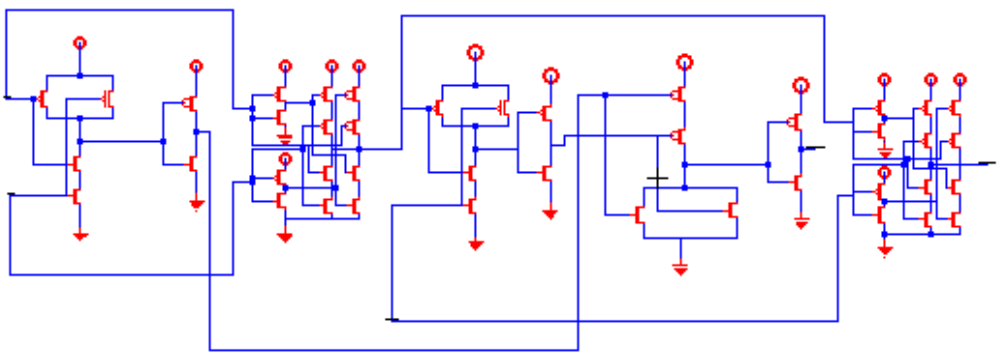

Figure 4 – Schematic of full adder.

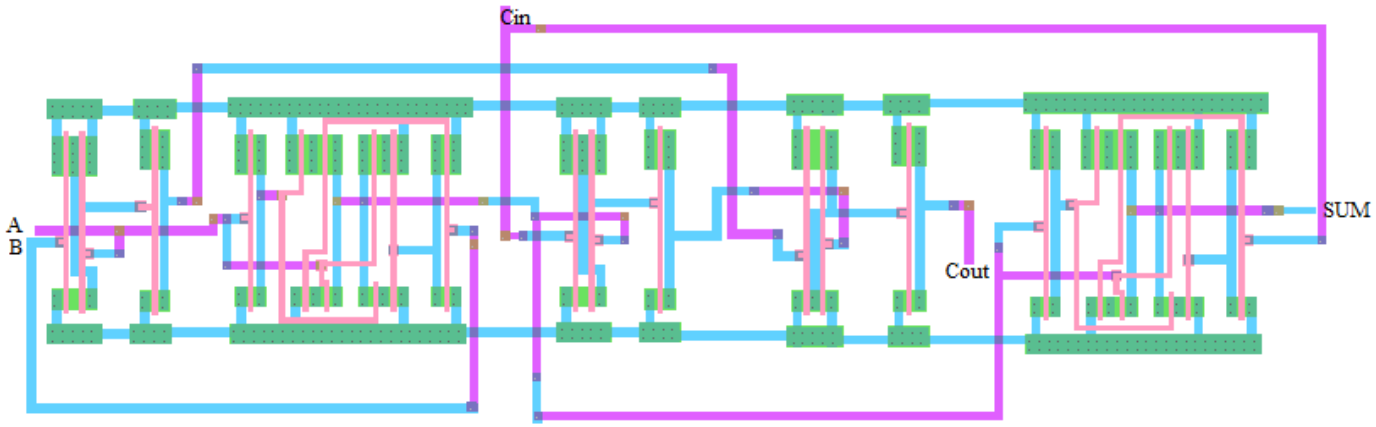

Figure 5 – Layout designing of full adder.

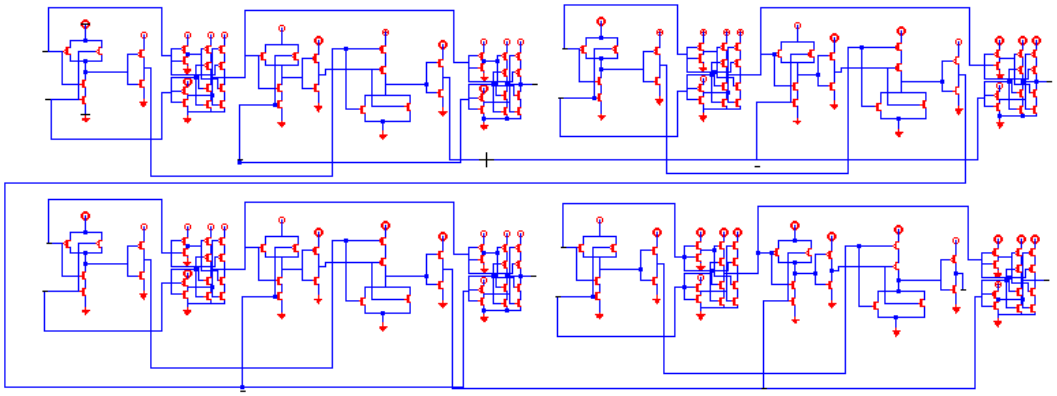

Figure 6 – Schematic of 4 bit CLA

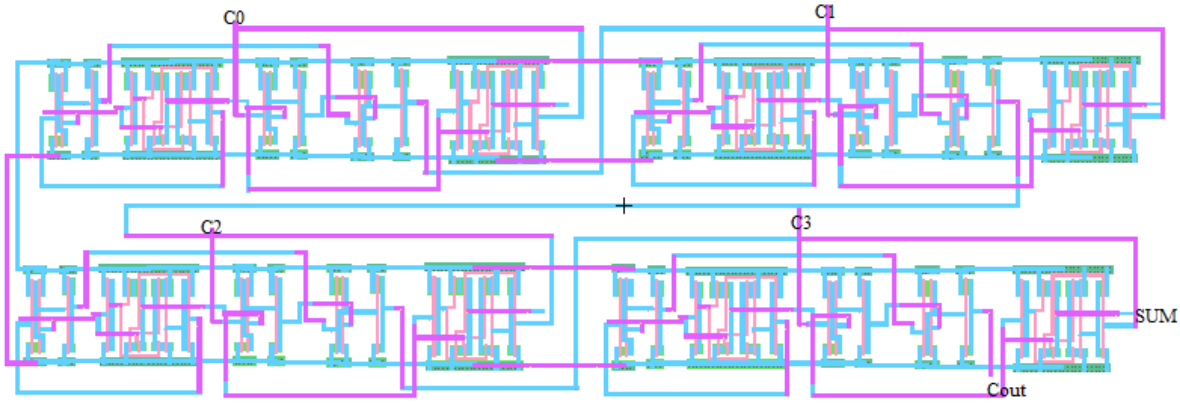

Figure 7 – Layout designing of 4 bit CLA.

Fig.5 shows the layout designing of full adder. Fig 7 shows the layout designing of 4 bit CLA.After designing of layout ,we will go for the transient analysis.

VI. CONCLUSION

We will get the output from the result of layout design, and through the simulation result we will go to analyze transient and frequency response of CLA.

In addition, open source Electric VLSI system is a user friendly that can be used for layout designing of very complex circuits. It is also possible with this software that we can cope with more complex circuit and find its transient response using IRSIM simulator.

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