Closed loop control of Thyristor Switched Capacitor (TSC) for instantaneous Reactive Power Compensation

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***Abstract*-- Development in electrical power transmission system and increased load demands require such systems that are very fast acting and reliable. Now-a-days Flexible AC Transmission Systems (FACTS) has become a subject of interest for the power system engineers. This technology eliminates the use of bulky, slow operating circuit breakers, and uses highly sophisticated semiconductor devices such as Thyristors, GTOs or IGBTs [1], [2], [3]. The closed loop control makes this system a very reliable which senses the voltage and frequency changes occurring in the system and take the remedial action instantaneously. The response time of this system is very less as compared to circuit breakers. In this paper, closed loop control of FACTS controller for shunt compensation is discussed and simulated using MATLAB 7.8. The load is increased and the response is checked for both open loop and closed loop control strategies. In closed loop control the voltage profile should be maintained, i.e. in-spite of abrupt load changes, the receiving end voltage should be within the prescribed limit. To maintain the voltage; the receiving end voltage is sensed and compared with the prescribed limit value, and then accordingly the compensation is carried out.**

Index Terms*— *Closed loop model, receiving end voltage (Vr) synchronized gate pulse, sending end voltage (Vs) and Thyristor Switched Capacitor (TSC).

I. INTRODUCTION

For any power system the main reason for deterioration of the voltage profile is the inductive (reactive) load. Due to this inductive load the reactive power comes into the picture and hence the voltage stability is lost. With the development of industries and increase in population, there is an increased demand in consumption of electrical power. For a power system to be termed as reliable it should not be affected by temporary overloads, i.e. Voltage should be constant with very less loss in transmission and distribution. Overload conditions should be compensated using appropriate compensators. There are mainly two types of compensation, viz. shunt and series. In series compensation, the overall line reactance is reduced by connecting a capacitor in series with the transmission line and hence voltage drop is reduced. In shunt compensation, reactive power is injected into the line so as to reduce the amount of reactive power supplied by source. Shunt compensation is a direct acting method which changes the receiving end voltages rapidly. It also improves the power factor. In this paper, shunt compensation method using FACTS controller is simulated. The FACTS controller used is Thyristor Switched Capacitor (TSC). It is connected or disconnected depending on the loading conditions and compensates the reactive power. The complete simulation is carried out in MATLAB 7.8 [11].

II. THYRISTOR SWITCHED CAPACITOR (TSC)

Thyristor switched capacitor is a capacitor that gets connected or disconnected to a transmission line through a pair of anti-parallel thyristors [4], [6]. The basic circuit is shown in Fig. 1 But this is not the actual circuit which is implemented. Suppose at an instant if TSC is on, then there will be very high di/dt, almost infinite. This can damage the thyristors. So to limit that, inductor is kept in series ensuring the protection of the thyristors as shown in Fig. 1. The waveforms for basic circuit are shown in Fig. 2.

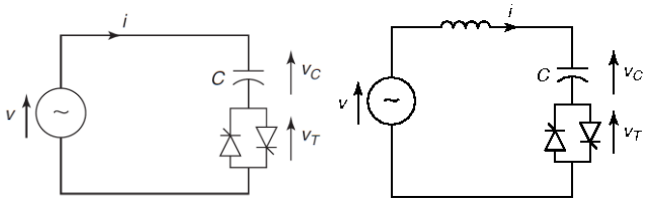


Fig.1. Basic & Actual Circuit of TSC

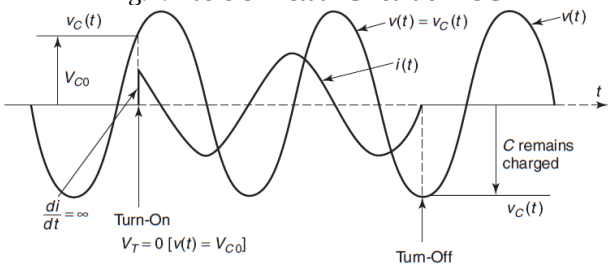


Fig.2. Waveform of TSC

As stated earlier, connecting a capacitor in parallel to the line will inject the reactive power into the system which in turn will result in power factor improvement and voltage compensation. This effect will improve the power quality and hence will make the system reliable. One more reason for selecting TSC as a shunt FACTS controller is that it does not inject any kind of harmonics into the system. The power transfer can be increased accordingly if same amount of current is to be taken from supply [7].

III. SIMULATION

The simulation circuit is shown in Fig. 3. The closed loop or open loop operation can be selected from the selector switch. Load is increased at 0.1s and hence the voltage at the receiving end reduces, which is to be compensated using the TSC model developed. The gate pulses generated for the TSC are synchronized with the supply. The advantage of these synchronized gate pulses is that they are instantly affected with any change in supply frequency, and hence keeps the

system in perfect synchronism without causing any unbalance due to abrupt switching during frequency changes. Normally a load of 2.4 MW is supplies by a 5km long transmission line. The transmission line is modeled as a pi-section. The load power factor is 0.8 lagging. The parameters of transmission line are R= 0.2720 Ω/km, L= 1.054e-3 Henry/km and C=1.12e-9 Farad/km.

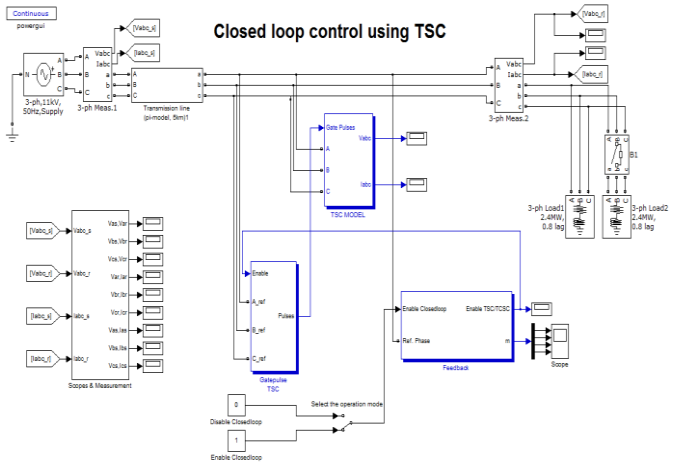


Fig.3 Simulation model for closed loop control of TSC

The TSC model developed in MATLAB is shown in Fig. 4.

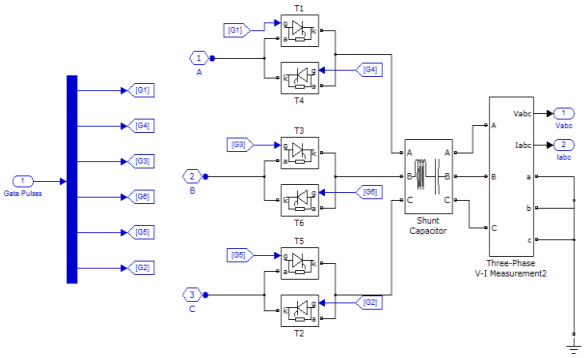


Fig.4 MATLAB Model of TSC

IV. RESULTS

A. GATE PULSES

Fig. 5 shows the synchronized gate pulses generated using the block developed in MATLAB. At 0.1s frequency of supply changes to 75Hz from 50Hz and it causes instantaneous change in the gate pulse width, this serves as an advantage to prevent false switching of the thyristor valves in TSC.

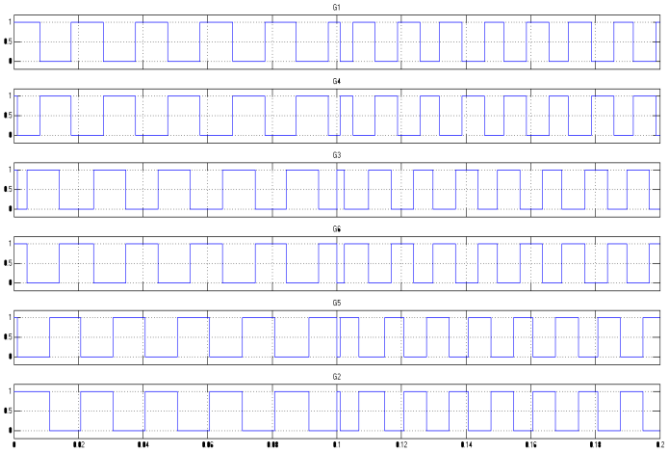


Fig. 5 Gate pulses generated at changing frequency for TSC

B. OPEN LOOP SIMULATION RESULTS

For open loop results, Fig. 6 shows the 3-phase receiving end voltages which decrease at 0.1s as the load increases.

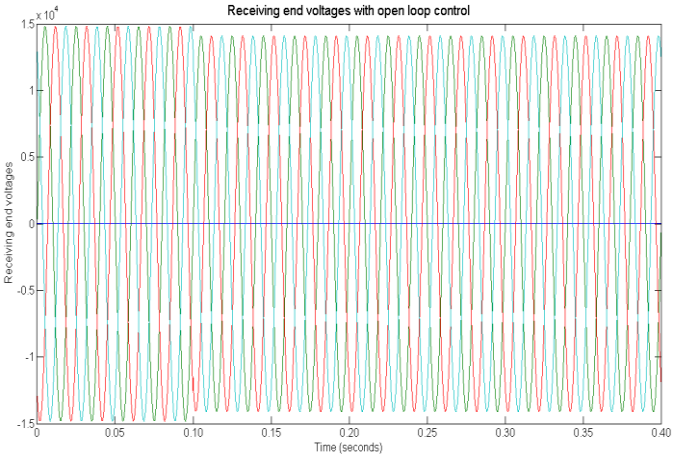


Fig. 6 Open loop results of receiving end voltages with increase in load

Fig. 7 shows the comparison of the sending and receiving end voltages of one phase. Voltage drop can be seen after 0.1s. Normally the receiving end voltage is lesser than the sending end voltage, but it is within the prescribed limits. Increasing the load decreases the voltage further going out of the limit and hence compensation is required at that time.

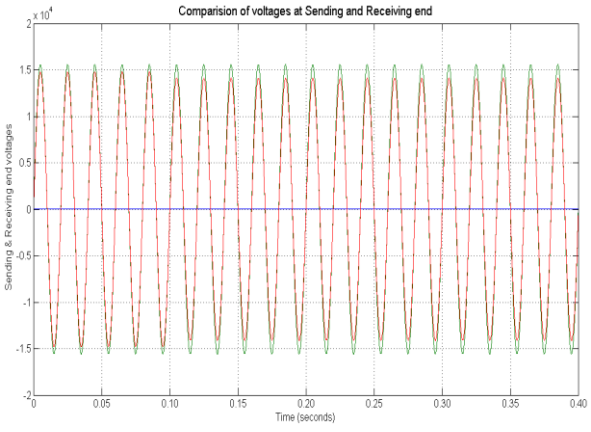
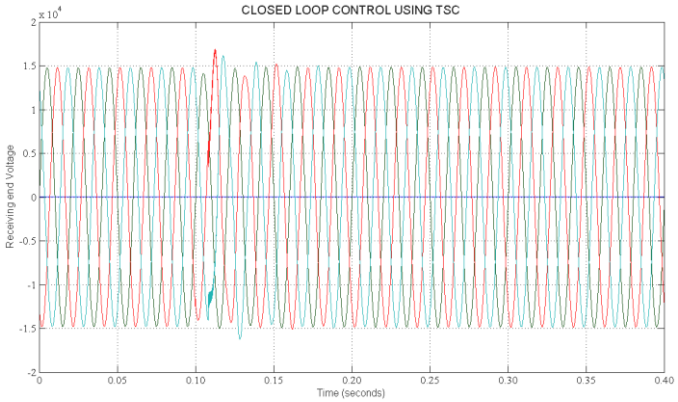


Fig. 7 Comparison of sending and receiving end voltages (Vs=green, Vr=red)

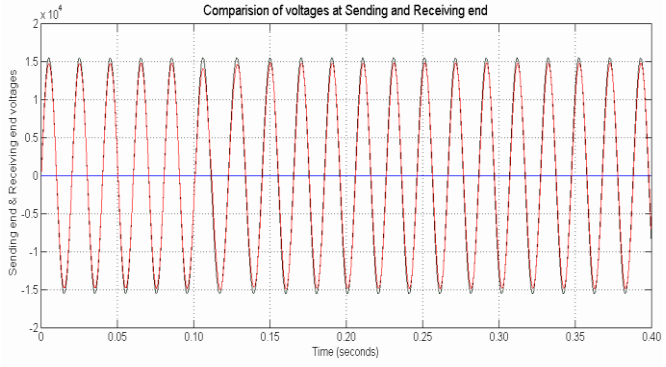
C. CLOSED LOOP SIMULATION RESULTS

For closed loop results, Fig. 8 shows the 3-phase receiving end voltages which decrease at 0.1s as the load increases. At 0.1s, although the load increases, the voltage is maintained constant after unbalance of 2 cycles. This shows the operation of the closed loop system. The closed loop block in the simulation circuit senses the voltage drop, compares it with the permitted drop value, and if it is lesser than the permitted value then it enables the TSC module hence starting the compensation which increases the voltage instantaneously. Hence the voltage is maintained at the same level even if the load is increased. This serves the purpose of maintaining the voltage profile better and hence retaining the power quality [7], [8], [9], [10].



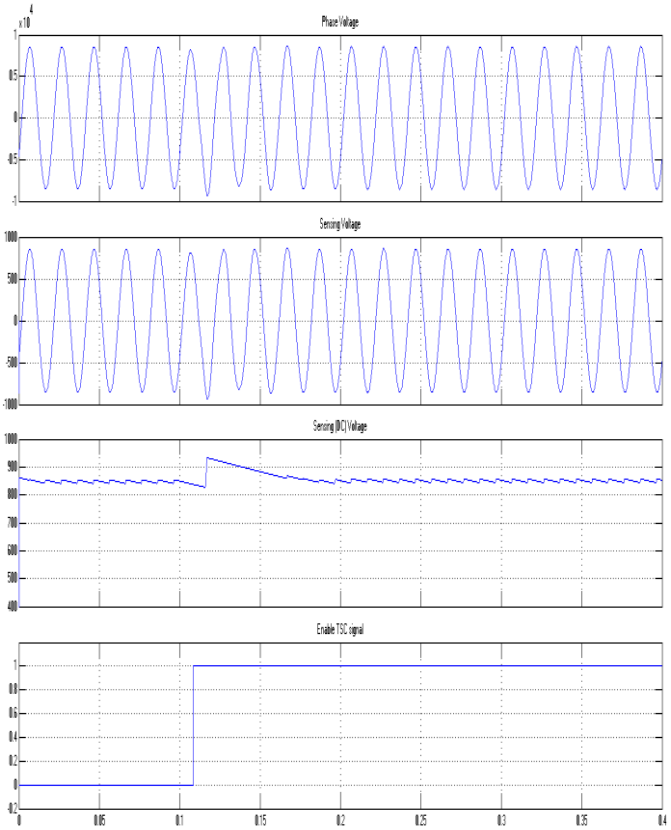
The reason for unbalance caused in the voltage is the capacitor entering the circuit. When the capacitor is connected, the phase voltages are not exactly zero and hence there is some unbalance in them. But after some time the voltages get balanced and maintained. The delay in sensing the overload is the main cause for this unbalance of the voltages.

Fig. 9 shows the comparison of the sending and receiving end voltages of one phase. Voltage drop cannot be seen after 0.1s due to the closed loop action which was visible in open loop Fig. 7.



D. CLOSED LOOP MODEL RESPONSE

The response of the closed loop model is shown in Fig. 10. The phase voltage is sensed using a potential transformer, that voltage is rectified and compared with a preset DC value. If the instantaneous DC value is lesser than the preset value, it indicates that the load has increased and compensation is required and hence TSC is enabled. This remains on until the load is connected.



E. COMPARISION OF CLOSED LOOP AND OPEN LOOP RESPONSE

For comparison, Fig 6 & 8 shows the receiving end voltages for dynamic load change. As the load increases at 0.1s; voltages drop for the open loop model while they are maintained constant for closed loop model. There is slight unbalance when the compensation comes in the circuit but that is eliminated within 2 cycles without affecting the system much. This unbalance occurs due to the capacitor getting connected into the circuit when voltages of all phases are not exactly zero. This causes the capacitor to charge instantaneously causing some unbalance.

V. CONCLUSION

From the results seen in Fig. 6, Fig. 7, Fig. 8 & Fig. 9, it can be seen that the voltage profile is maintained well for rapid load changes. This serves the purpose of a reliable power system, that receiving end voltages should not be changes in spite of load changes. Although there is some unbalance in the system during the switching of the compensators, but that does not affect the system too much. The system is continuously monitored for voltage and frequency changes. The closed loop block continuously monitors the voltage and the synchronized gate pulse block continuously monitors the frequency. According to the changes in the system, the control is achieved to maintain the voltage profile constant and provide a better quality power to the consumers. The advantage of this system is that it is a very fact acting system, rapidly changes the voltages. Also TSC used does not inject any kind of harmonics into the system hence further maintaining the power quality.

REFERENCES

[1] John J. Paserba," How FACTS Controllers Benefit AC Transmission Systems", IEEE 2003.

[2] Brian K. Johnson, "Benchmark Systems for Simulation of TCSC and SVC", IEEE Transaction, 2002.

[3] R.K.Verma, R.M.Mathur, "Thyristor-based facts controllers for electrical transmission systems", IEEE Press, pages 277-288, 2002.

[4] Jonathan (Jon) Berge and Rajiv K. Varma, "Design and Development of a Static VAR Compensator for Load Compensation Using Real-Time Digital Simulator and Hardware Simulation", IEEE Transaction 2007.

[5] Lutz Kirschner and Gerhard H. Thumm, "Design and experience with Thyristor controlled and Thyristor protected series capacitor", IEEE Transaction 2002.

[6] Rahmatollah Hooshmand, Mehdi Torabian Esfahani2 Arash Kiyoumarsi, " Design of Parallel TSC for Reactive power compensation in Electric Arc Furnaces", Proceedings of the 2008 International Conference on Electrical Machines.

[7] Shankaralingappa C. B., and Suresh. H. Jangamashetti," FACTS Controllers to Improve Voltage Profile and Enhancement of Line Loadability in EHV Long Transmission Lines", IEEE Transaction 2008.

[8] H. K. Tyll," FACTS Technology for Reactive Power compensation and System Control", 2004 IEEE IPES Transmission & Distribution Conference & Exposition .

[9] Rolf Grünbaum and Mikael Halonen, "SVC for 69 kV Direct Grid Connection", IEEE Transaction, 2008.

[10] T.Vijayakumar, A.Nirmalkumar and N.S. Sakthivelmurugan, "Reactive Power Control Using FC - TSR - TCR", Research Journal of Applied Sciences, Engineering and Technology 2(1): 1-4, 2010 ,ISSN: 2040-7467

[11] Software package : MATLAB 7.8(R2009a) + Simulink

[10] John J. Paserba, "How FACTS Controllers Benefit AC Transmission Systems", IEEE 2003.

[11] Yan Ou, Chanan Singh, "Improvement of Total Transfer Capability Using TCSC and SVC", IEEE 2001.

[12] Belkacem Mahdad, Tarek Bouktir, Kamel Srairi, "Strategy of Location and Control of FACTS Devices for Enhancing Power Quality", IEEE 2006.

[13] N.G.Hingorani, Laszlo Gyugyi, "Understanding FACTS", IEEE Press, 2001, pp 225-235.

[14] R.M.Mathur, R.k.Verma, "Thyristor-based FACTS controllers for electrical transmission systems", IEEE Press, 2002, pp 277-288.