Step-Up DC-DC Converter with High Voltage Gain Using Switched-Inductor Technique

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***Abstract*- A simple dc-dc boost converter are unable to provide high step-up voltage gains due to the effect of power switches, rectifier diodes, and the equivalent series resistance of inductor and capacitors. In this paper proposes new dc-dc converter to achieve high voltage gain without an extremely high duty ratio. In the proposed converters, two inductors with the same level of inductance are charged in parallel during the switch –on period and are discharged in series during the switch-off period. In this converter mainly proposed converter. That is used for PV system and DG systems.**

Keywords — dc-dc boost converter, high step-up voltage gain, power stage, without an extremely high duty ratio.

I. INTRODUCTION

DC–DC converter with a high step-up voltage gain is used for many applications, such as high intensity discharge lamp ballasts for automobile headlamps, fuel-cell energy conversion systems, solar-cell energy conversion systems, and battery backup systems for uninterruptible power supplies. Theoretically, a dc–dc boost converter can achieve a high step-up voltage gain with an extremely high duty ratio [5]–[6]. However, in practice, the step-up voltage gain is limited due to the effect of power switches, rectifier diodes, and the equivalent series resistance (ESR) of inductors and capacitors. Moreover, the extremely high duty-ratio operation will result in a serious reverse-recovery problem. Many topologies have been presented to provide a high step-up voltage gain without an extremely high duty ratio[8,9].

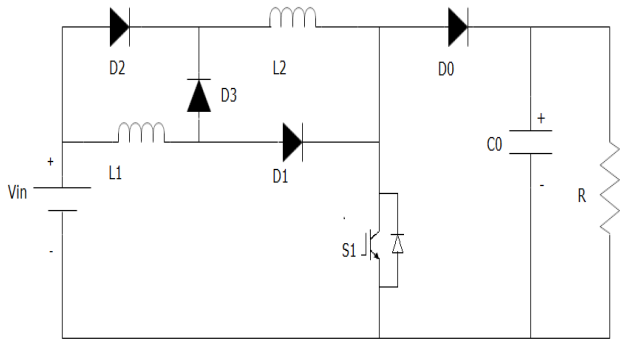


Figure (1) basic proposed boost converter

The coupled-inductor techniques provide solutions to achieve a high voltage gain, a low voltage stress on the active switch, and a high efficiency without the penalty of high duty ratio [5]–[9].

Literature includes some research of the proposed dc–dc converters, which include the cascade boost type [3], the quadratic boost type [10], the voltage-lift type [11], the capacitor-diode voltage multiplier type [6], [4], and the boost type integrating with switched-capacitor technique [13]. However, these types are all complex and have a higher cost. The modified boost type with switched-inductor technique is shown in Fig. 1 [13]. The structure of this converter is very simple. Only one power stage is used in this converter. However, this converter has two issues:1) Three power devices exist in the current-flow path during the switch-on period, and two power devices exist in the current flow path during the switch-off period, and 2) the voltage stress on the active switch is equal to the output voltage. A new dc–dc high step-up converter is proposed in this paper, as shown in Fig. 2(a). Compared with the converter in [13], the proposed converter I has the following merits:

1) Two power devices exist in the current-flow path during the switch-on period, and one power device exists in the current flow path during the switch-off period; 2) the voltage stresses on the active switches are less than the output voltage; and 3) Under the same operating conditions, including input voltage, output voltage, and output power, the current stress on the active Switch during the switch-on period is equal to the half of the current stress on the active switch of the converter in [13]. For getting higher step-up voltage gain, the other dc–dc converters are also presented in this paper, as shown in Fig. 2(b) and (c). These three proposed dc–dc converters utilize the switched inductor technique, in which two inductors with same level of inductance are charged in parallel during the switch-on period and are discharged in series during the switch-off period, to achieve high step-up voltage gain without the extremely high duty ratio. The operating principles and steady-state analysis are discussed in the following sections. To analyse the steady state characteristics of the proposed converters, some conditions are assumed as follows: 1) All components are ideal—the ON-state resistance *R*DS(ON) of the active switches, the forward voltage drop of the diodes, and the ESRs of the inductors and capacitors are ignored—and 2) all capacitors are sufficiently large, and the voltages across the capacitors can be treated as constant.

II. IMPROVEMENT OF BOOST CONVERTER

This topology is similar to the basic one except for adding two voltage lift circuits. shows this improved topology Figure (2). In fact, this converter uses two inductors of the same inductance level, and the two switches being simultaneously. Similarly to the other converter circuits, the operation of such a converter is subdivided into two modes; The CCM and the DCM. Typical waveforms of these modes are depicted in Figure (3). The following subsections address the performance and steady state analysis of this converter [14].

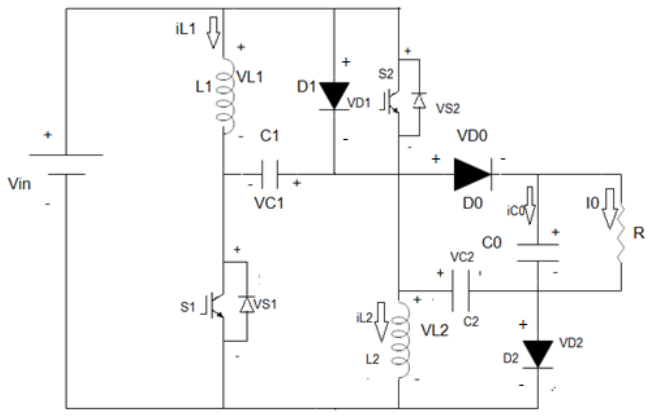


Figure (2) the circuit diagram of improved topology

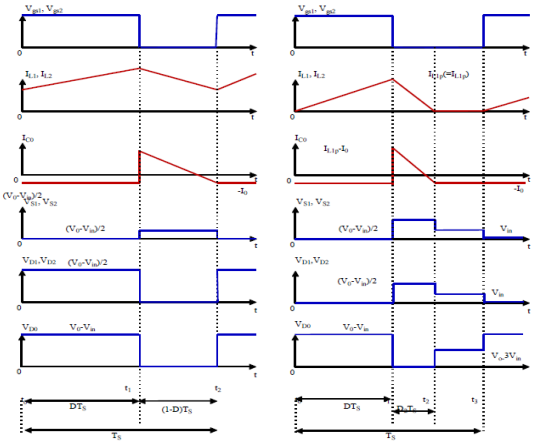


Figure (3) typical voltage and current waveform for improved topology [14]

The Continuous Conduction Mode (CCM)

This mode of operation can be further divided into two stages:

STAGE 1: This stage extends from t_0 to t_1. In this interval, switches $S_1$and S_2 and are both turned on shown in figure (3-a). During this stage, inductors L_1 and L_2 are charged in parallel from the DC source whereas the capacitor C_0 releases its energy to the load. Moreover, capacitors C_1 and C_2 are charged from the DC source[14].

The voltages across L1, L2, C1 and C2 are given by:

$$V_{L1} = V_{L2} = Vin = V_{L2} = V_{c2} \quad \text{.....(1)}$$

STAGE 2: which extends from t1 to t2 shown in figure (3-a). During this time interval, S_1 and S_2 switched off as shown in the equivalent circuit shown in Figure 2. Besides,L_1 L_2,C_1 and C_2 are connected in series to the DC source in order to transfer the stored energy to C_0 and the load. So, the voltages across L_1 and L_2 are derived as:

$$V_{L1}=V_{L2}=\frac{Vin+Vc1+Vc2-V0}{2} = \frac{3Vin-Vo}{2} \quad \text{.....(2)}$$

The two inductors are equal in values and have the same current implies the condition in (2).doing the integration in (2), The voltage gain can be evaluated as in (3);

$$\int_0^{DTs} Vin\ dt + \int_{DTs}^{Ts} \frac{3Vin-V0}{2}\ dt = 0 \quad \text{.....(3)}$$

The voltage gain is thus derived by (3) rearranging

$$\frac{V0}{Vin} = \frac{3+D}{1-D} \quad \text{.....(4)}$$

The voltage gain in (6) is plotted versus duty cycle (D) in Figure 4.

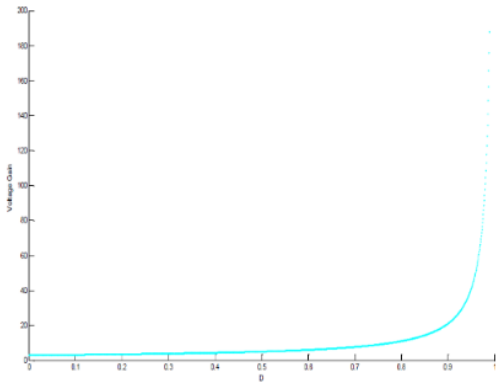


Figure (4) Voltage Gain versus Duty Cycle for the improved Topology in the CCM of the improved Topology [14]

D is the duty cycle;

The voltage of the switches S_1 and S_2 is given by:

$$V_{s1} = V_{s2} = V_{D1} = V_{D2} = \frac{V0-Vin}{2} \quad \text{.....(5)}$$

The diode voltage is,

$$V_{D0} = V0\text{-}Vin \quad \text{.....(6)}$$

The Discontinuous Conduction Mode (DCM)

The DCM is also subdivided into three distinct stages:

STAGE1: This takes place between t_0 and t_1 shown in fig.(3-b). The status of the converter is the same as that of stage 1 in the CCM. During this stage the converter will have the equivalent circuit shown in figure (2).

The peak currents of inductors L1 and L2 can be found as,

$$I_{L1p} = I_{L2p} = \frac{Vin}{L} DTs \quad \text{.....(7)}$$

STAGE 2: This extends from t1 to t2 shown in fig.(3-b). In this time interval, the switches S_1 and S_2 are turned off, the inductors L_1 and L_2 and capacitors C_1 and C_2 are series connected with the DC source in order to transfer the stored energy to the capacitor C_0 and the load.[14]

The inductor currents I_{L1p} and I_{L2p} start decreasing to zero at t=t2. Another expression for IL1p and IL2p is that of (8).

$$I_{L1p} = I_{L2p} = \frac{V0-Vin-VC1-VC1}{2L} D2Ts \quad \text{.....(8)}$$

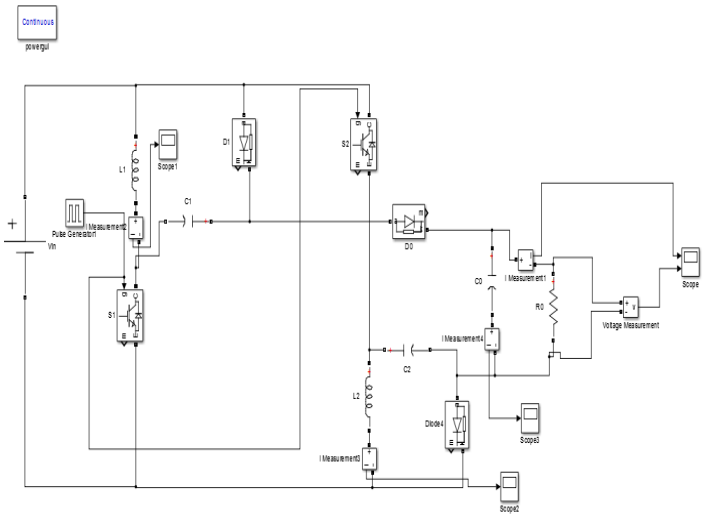
$$I_{L1p} = I_{L2p} = \frac{V0-3Vin}{2L} D2Ts \quad \text{.....(9)}$$

STAGE 3: Which occurs between t2 and t3 shown in fig.(3-b). During this time interval, S_1 and S_2 are still turned off, on the capacitor C_o charges the R-load since the energy in L_1 and L_2 is zero [14].

Rearranging (9) and substituting (8),one can write:

$$D_2 = \frac{2DVin}{V0-3Vin} \quad \text{.....(10)}$$

Observing the waveform of Ic0 in fig(3-b) ,the The average value of the capacitor output current during the whole period is found as follows:



$$I_{C0} = \frac{\frac{1}{2}D2TsIL1p-I0Ts}{Ts} = \frac{1}{2}D2\ IL1p - I0 \quad \text{.....(11)}$$

Substituting,(10) and (11) in (12), the result is:

$$I_{C0} = \frac{D^2Vin^2Ts}{L(Vo-3Vin)} - \frac{V0}{R} \quad \text{.....(12)}$$

The capacitor output current equal zero, so;

$$I_{C0} = \frac{D^2Vin^2Ts}{L(Vo-3Vin)} - \frac{V0}{R} = 0 \quad \text{.....(13)}$$

Or equivalently:

$$\frac{D^2Vin^2Ts}{L(Vo-3Vin)} = \frac{V0}{R} \quad \text{.....(14)}$$

The voltage gain in this stage is given by:

$$\frac{V0}{Vin} = \frac{3}{2} + \sqrt{\frac{9}{4} + \frac{D^2}{Tl}} \quad \text{.....(15)}$$

Based on (15), Figure (5) shows a plot of the voltage gain versus duty cycle in the discontinuous mode.

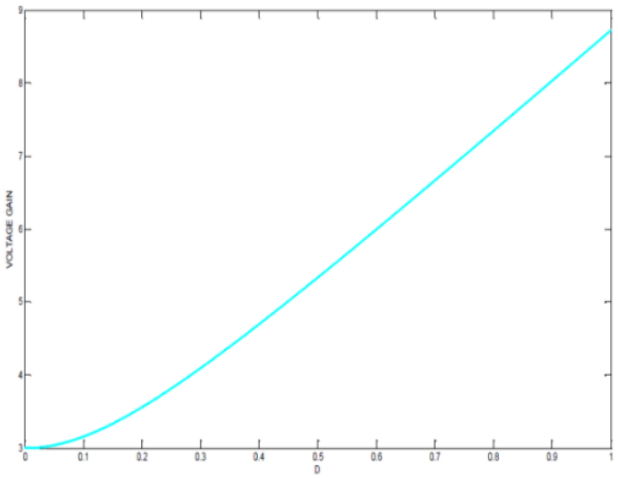
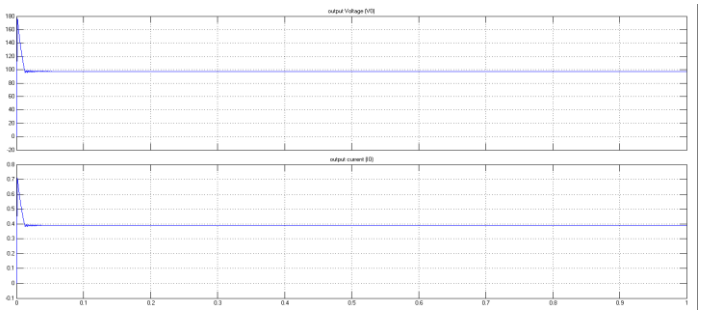


Figure (5) Voltage Gain versus Duty Cycle for the improved Topology in the DCM of the improved Topology [14]

III. SIMULATION RESULT



IV. COMPARISON WITH DIFFERENENT DUTY CYCLE OF PROPOSED CONVERTER

Duty cycle	Vin	Iin	Vout	Iout	Pin	Pout	Efficiency(%)
0.1	12	1.21	37.89	0.155	14.5	5.87	40.54
0.2	12	1.36	41.2	0.172	16.35	7.09	43.38
0.3	12	1.38	45.33	0.18	16.5	8.16	48.98
0.4	12	1.39	50.9	0.21	16.66	10.89	64.8
0.5	12	1.6	58.93	0.24	19.23	14.14	73.5
0.6	12	1.95	70.43	0.29	23.4	20.42	87.9
0.7	12	3.04	91.32	0.37	36.5	33.79	92.7
0.8	12	6.45	130.9	0.55	77.4	71.99	93.8
0.9	12	21.1	251.33	0.99	255.7	248.8	97.3

V. CONCLUSION

This paper has studied novel dc–dc converters with high step-up voltage gain. The structures of the proposed converters are very simple. Since the voltage stresses on the active switches are low, active switches with low voltage ratings and low ON-state resistance levels RDS (ON) can be selected. In this paper we can analyse different duty with efficiency and voltage gain. The simulation results confirm that high step-up voltage gain can be achieved.

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