# Multilevel Inverter For High Voltage Applications

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***Abstract* - This paper gives a diagram of a single-phase seven-level inverter for grid-connected photovoltaic frameworks, with a novel pulse width-modulated (PWM) control conspire. Three reference signals that are comparative to each other with a counterbalanced that's identical to the sufficiency of the triangular carrier flag were utilized to create the PWM signals. The inverter can think of the seven degrees of yield voltage levels (Vdc, 2Vdc/3, Vdc/3, 0, −Vdc, −2Vdc/3, −Vdc/3) from the dc supply voltage. A control plot is executed microcontroller PIC16F877A. The proposed framework was verified by actualizing in a model.**

***keywords* - Grid associated modulation index, multilevel inverter, photovoltaic (PV) system, total harmonic distortion (THD).**

## I. INTRODUCTION

The ever-increasing vitality utilization, fossil fuels rising costs and expendable nature, and getting to be more regrettable worldwide environment have made a growing interested in sustainable energy time systems, one of which is photovoltaic. To produce power, the sun's vitality is changed over into power by this framework. The power system network takes generated photovoltaic energy through network associated inverter.

For the most part, for private or low-power applications of power ranges less than 10 kW, a single-phase grid-connected inverter is ordinarily utilized [1]. Sorts of single-arrange grid associated inverters have been found [2]. Full-connect three-level could be a general topology of this inverter. Exceptionally high switching fulfills the determination of three level inverter, but it seem moreover tragically increment switching losses, acoustic noise, and level of obstructions to other equipment. The consonant content are diminished so there's enhancement in yield voltage, subsequently, moreover the measure of the filter utilized and the level of electromagnetic interference (EMI) made by the inverter's trading activity [3].

Multilevel inverters create yield voltage as a sinusoidal waveforms, yield current with more desirable harmonic consider, less weight of electronic components tends to diminished voltages, exchanging losses which are lower than those of ordinary two-level inverters, a miniature filter size, and lesser EMI, all of these make them less in cost, lighter, and more compact; so multilevel inverters are favorable [3], [4].

Over the long time different topologies for multilevel inverters have been proposed. These are diode-clamped [5]–[10], flying capacitor or multicell, cascaded H-bridge, and adjusted H-bridge multilevel.

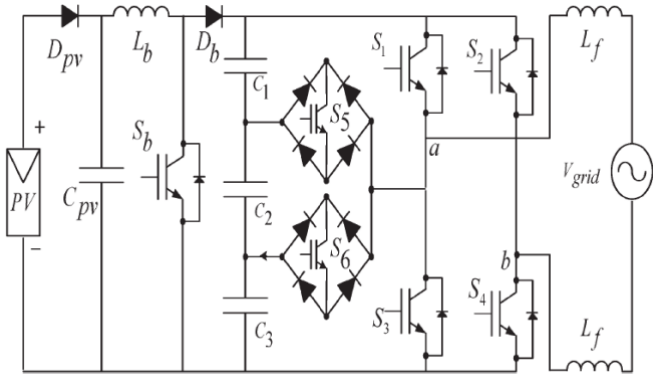



Fig.1.Proposed single-stage seven-level grid-connected inverter for the photovoltaic systems

The progress of a novel modified H-bridge single-stage multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) method has relates by this paper. With contemplations for a maximum-power-point tracker (MPPT) and a current-control calculation the topology was connected to a grid-connected photovoltaic framework.

## II. PROPOSED MULTILEVEL INVERTER TOPOLOGY

In [25]–[29] the single-stage seven-level inverter was produced from the five-level inverter. As appeared in Fig. 1 it include a single stage ordinary H-bridge inverter, two bidirectional switches, and a capacitor voltage divider framed by C1, C2, and C3. The topologies, i.e., less power switch, power diodes, and less capacitor for inverters of the same number of levels, the adjusted H-bridge topology is essentially useful.

Through a dc–dc boost converter, photovoltaic (PV) arrays were related to the inverter. The control network gets the power which is produced by the inverter, so the utility grid, instead of a stack, was utilized. The PV arrays had a voltage that was lesser than the grid voltage since of that dc-dc boost converter is required. To guarantee that power streams from the PV arrays to the grid, more dc bus voltage are vital. To filter the current infused into the network a filtering inductance Lf was utilized. Seven yield-voltage levels can made by genuine switching of the inverter (Vdc, 2Vdc/3, Vdc/3, 0, −Vdc, −2Vdc/3, −Vdc/3) from the dc supply voltage.

As appeared in Fig. 2(a)–(g) the favored inverter's operation can be isolated into seven switching states. A conventional inverter's operational states in grouping is appeared in Fig. 2(a), (d), and (g), however extra states inside the proposed inverter organizing one-and two-third degrees of the dc-bus voltage is showed up by Fig. 2(b), (c), (e), and (f).

The indicated seven levels of output voltage were produced as follows

1) Positive most extreme output (Vdc): By connecting the load positive terminal to Vdc, S1 is ON and by connecting the load negative terminal to ground, S4 is ON. All other controlled switches are OFF; the voltage provided to the load terminals is Vdc. The current ways that are active at this stage are appeared by fig. 2(a).

2) Two-third positive yield (2Vdc/3): By connecting the load positive terminal, the bidirectional switch S5 is ON, and by connecting the load negative terminal to ground, S4 is ON. The voltage connected to the load terminals is 2Vdc/3, all other controlled switches are OFF; the current ways that are active at this stage are appeared by Fig. 2(b).

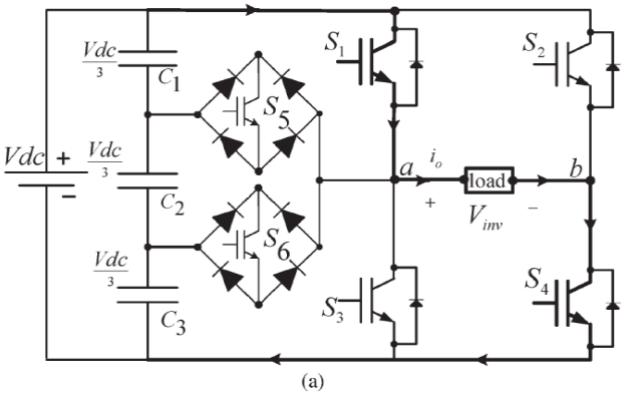
3) One-third positive yield (Vdc/3): By connecting the load positive terminal, the bidirectional switch S6 is ON and by connecting the load negative terminal to ground, S4 is ON. All further controlled switches are OFF; the voltage connected to the load terminals is Vdc/3. The current ways that are active at this arrange are appeared by fig 2(c).

4) Zero yield: The zero level can be created by two switching blends; S1 and S2 are ON, or switches S3 and S4 are ON, and all other controlled switches are OFF; the voltage connected to the load terminals is zero and terminal ab is a short circuit. The current ways that are active at this stage are appeared in Fig. 2(d).

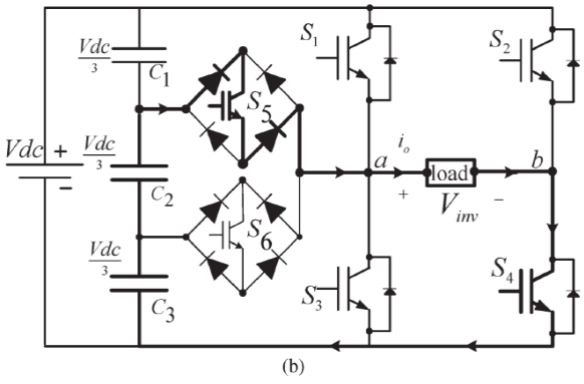
5) Negative one-third yield (−Vdc/3): For connecting the load positive terminal, the bidirectional switch S5 is ON and for connecting the load negative terminal to DC, S2 is ON. The voltage connected to the load terminals is −Vdc/3; All other controlled switches are OFF. The current ways that are active at this stage are appeared by fig 2(e).

6) Negative Two-third yield (−2Vdc/3): By connecting the load positive terminal, the bidirectional switch S6 is ON and by connecting the load negative terminal to ground, S2 is ON. The voltage connected to the load terminals is −2Vdc/3; all other controlled switches are OFF. The current ways that are active at this stage are appeared by Fig. 2(f).

7) Negative most extreme yield (−Vdc): For connecting the load negative terminal to Vdc, S2 is ON and for connecting the load positive terminal to ground, S3 is ON. The voltage associated to the load terminals are –Vdc; all other controlled switches are OFF. The current ways that are active at this stage are appeared by Fig 2(g).



(a)



(b)

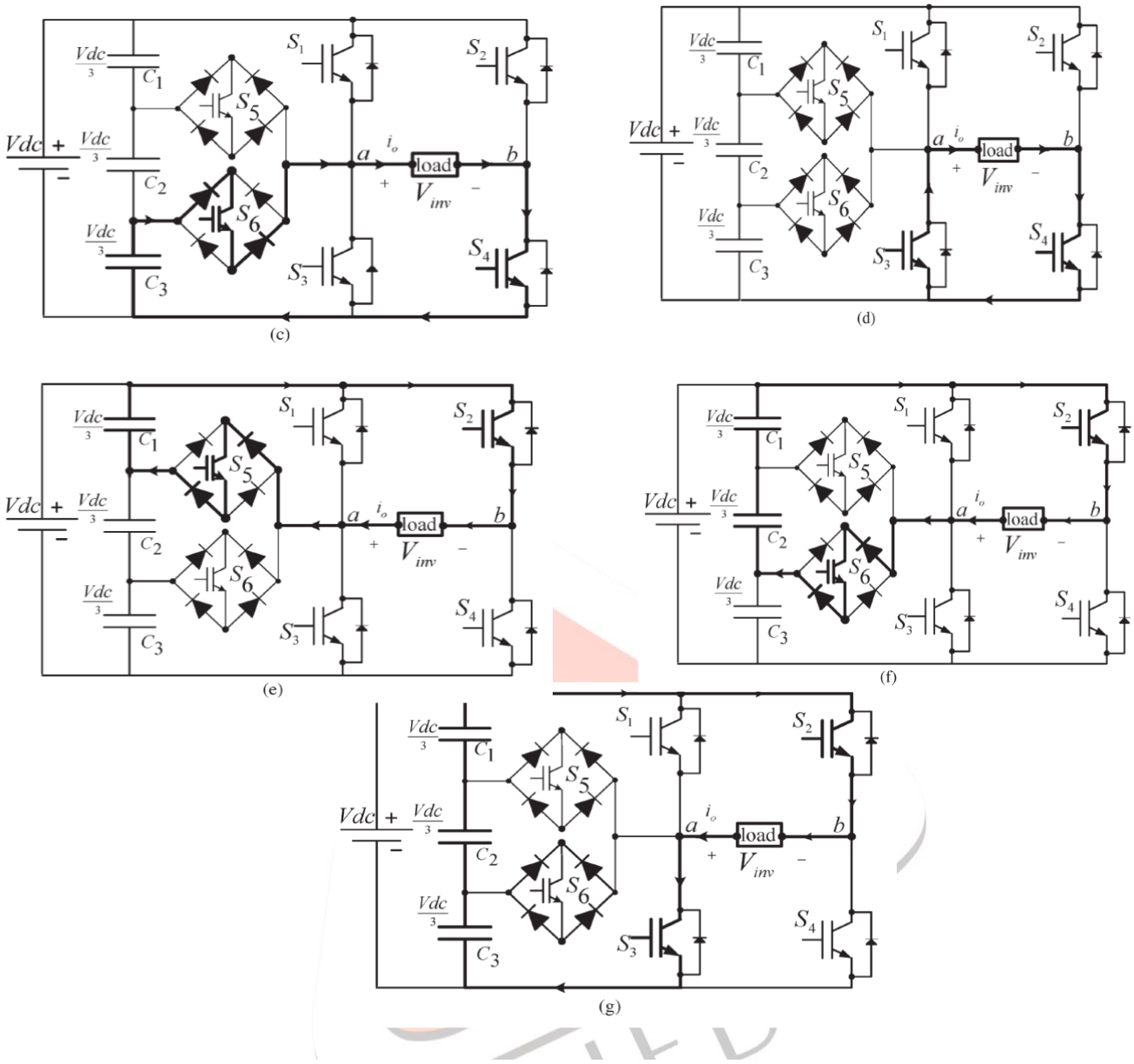


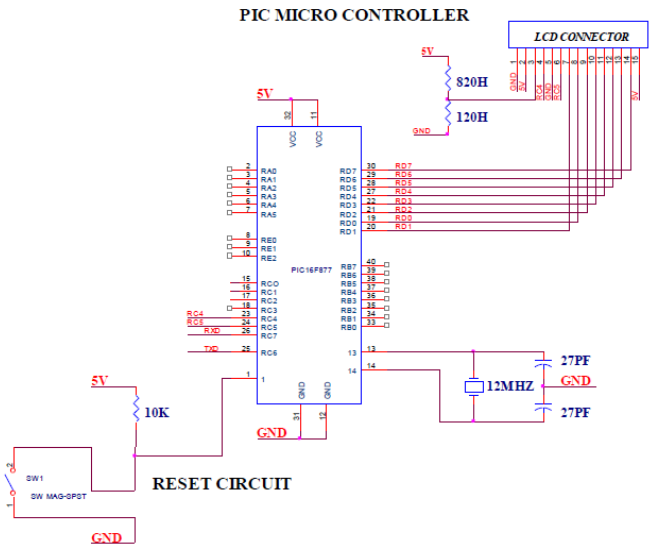

Fig.2. Switching combination required to produce the output voltage (Vab).(a) Vab = Vdc. (b) Vab = 2Vdc/3. (c) Vab= Vdc/3. (d) Vab= 0(e) Vab = −Vdc/3. (f) Vab= −2Vdc/3. (g) Vab = −Vdc

OUTPUT VOLTAGE ACCORDING TO THE SWITCHES' ON–OFF CONDITION

| $v_0$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ |
|---|---|---|---|---|---|---|
| $V_{dc}$ | on | off | off | on | off | off |
| $2V_{dc}/3$ | off | off | off | on | on | off |
| $V_{dc}/3$ | off | off | off | on | off | on |
| 0 | off | off | on | on | off | off |
| 0* | on | on | off | off | off | off |
| $-V_{dc}/3$ | off | on | off | off | on | off |
| $-2V_{dc}/3$ | off | on | off | off | off | on |
| $-V_{dc}$ | off | on | on | off | off | off |

Table I indicates the switching mixes that generated the seven output-voltage levels (0, −Vdc, −2Vdc/3, −Vdc/3, Vdc, 2Vdc/3, Vdc/3).

CONTROL SYSTEM




**CORE FEATURES:**

• High-execution RISC CPU
• Only 35 single word guidelines to retain
• All single cycle guidelines aside from program branches which are two cycle
• Operating rate: DC - 20 MHz clock input
DC - 200 ns guidance cycle
• Up to 8K x 14 expressions of Flash Program Memory,
Up to 368 x 8 bytes of Data Memory (RAM)
Up to 256 x 8 bytes of EEPROM information memory
• Pin out good to the PIC16C73/74/76/77
• Interrupt ability (up to 14 inward/outside
• Eight level profound equipment stack
• Direct, circuitous, and relative tending to modes
• Power-on Reset (POR)
• Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
• Watchdog Timer (WDT) with its own on-chip RC Oscillator for solid activity
• Programmable code-assurance
• Power sparing SLEEP mode
• Selectable oscillator choices
•Low-power, fast CMOS EPROM/EEPROM innovation
• Fully static structure
• In-Circuit Serial Programming (ICSP) by means of two pins
• Only single 5V source required for program ability
• In-Circuit Debugging via two pins
• Processor read/compose approach to program memory
• Wide working voltage goes: 2.5V to 5.5V
• High Sink/Source Current: 25 mA
• Commercial and Industrial temperature ranges
• Low-power utilization:
< 2mA run of the mill @ 5V, 4 MHz
20mA run of the mill @ 3V, 32 kHz
< 1mA run of the mill reserve current

**PERIPHERAL FEATURES:**

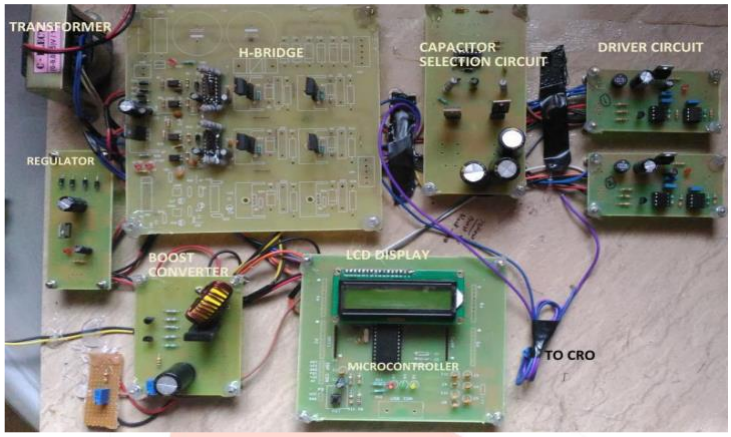
• Timer0: 8-piece clock/counter with 8-piece prescaler
• Timer1: 16-piece clock/counter with prescaler, can be expanded during rest
Through outside precious stone/clock
• Timer2: 8-piece clock/counter with 8-piece period register, prescaler and postscaler
• Two Capture, Compare, PWM modules
Catch is 16-piece, max goals is 12.5 ns,
Analyze is 16-piece, max goals is 200 ns,
PWM max. Goals is 10-piece
• 10-piece multi-channel Analog-to-Digital converter
• Synchronous Serial Port (SSP) with SPI. (Ace Mode) and I2C. (Ace/Slave)
• Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with

9-Bit tends to identification.

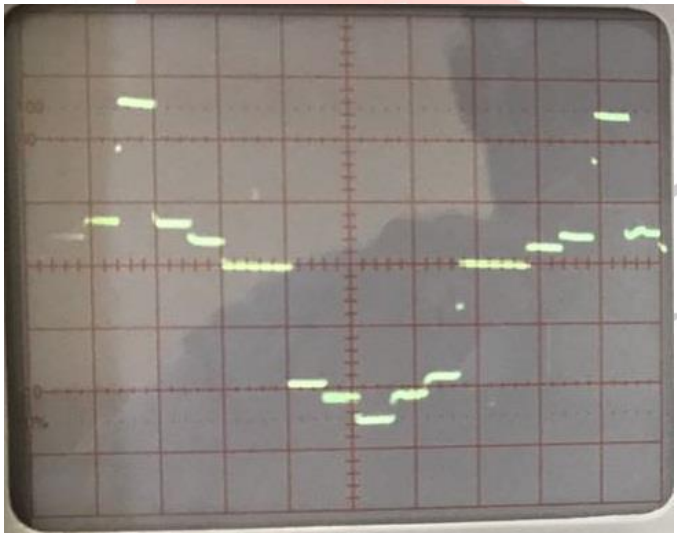
V. SYSTEM PARAMETERS

| Sr. no | Name of parameter | Specifications |
|---|---|---|
| 1 | Microcontroller | PIC16F877A |
| 2 | Transformer | 230/15V |
| 3 | Voltage regulator | IC7805,7812,7815 |
| 4 | MOSFET | IRF840-200V,3A |
| 5 | LCD display | 16*2 |
| 6 | Driver circuit | IC7667,0-15V,1A |

VI. HARDWARE CONFIGURATION




VII. HARDWARE RESULTS



VIII. RESULT DESCRIPTION

1. Output of boost converter is 24 V dc which is double of that of supply voltage.
2. Peak voltage present at the output of inverter is 24V.
3. Output by capacitor selection circuit is step like and hence approximated to sinusoidal.

IX. REFERENCES

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