Design of dexterous VLSI architecture of FFT using verilog

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Abstract— Fast Fourier Transform (FFT) having a considerable impact on the performance of communication system has been a hot topic of research for many years. Fixed point numbers are most widely involved in FFT computation, in which the accuracy is one of the most important backlogs. Thus the floating point operation was included in butterfly unit. However, FP butterfly architecture has the main disadvantage is slow as compared with the fixed point computation. In this paper, the floating point fused dot product unit is used for latency reduction. Efficient Radix8 butterfly unit with FDPA was proposed. This butterfly unit performs faster than the conventional butterfly. Finally, the performance analysis of various Radix architectures such as Radix2, Radix4 and Radix8 are shown. Radix8 requires less number of adders and multipliers when compared to the other lower order radices. Thus the Radix8 architecture was chosen, in which the FDPA algorithm was implemented. Hence the speed of FFT computation with FP multiplier can be enhanced.

IndexTerms— Fused Dot Product Add (FDPA), Fast Fourier Transform (FFT), Floating Point multiplier (FP).

I. INTRODUCTION

Traditional Fast Fourier Transform (FFT) plays a great role in various applications such as OFDM, Filtering, spectral analyzer, Radar etc. The FFT computation is carried out by resolving the butterfly units. The major task is to include the floating point operation in FFT architecture. There are various FFT Radix architectures are available. The number of multipliers and adders required for the various Radix structures are varied. Thus the efficient Radix8 structure was chosen in which the floating point operation was included. But the latency rose tremendously when compared to the traditional Radix8. Hence, the enhanced multiplication technique called FDPA is used. By using XILINX and ModelSim, the dexterous VLSI architecture of FFT was implanted. In addition to that, the comparison between the various Radix architectures in terms of Timing constraints is shown. The performance analysis gives the complete information about the proposed system speed improvement.

II. BASIC RADIX2 ARCHITECTURE

In 1965, Fast Fourier Transform was developed by J.W.COOLEY and J.W.TUCKEY. The FFT is based on decomposition and breaking the samples into smaller units and combining them to obtain the frequency domain signal. First, here is the simplest butterfly. It’s the basic unit, consisting of just two inputs and two outputs. If N is power of 2, it can divide DFT and more. Finally, it divide several DFT (butterfly computation) of N=2.

![Figure 1: Radix2 Butterfly Diagram](image1)

Similarly, there are various butterfly units with different Radices are shown as below. In Radix4, four inputs and four outputs are available. Let us consider N be the number of samples, then it is splitted as N/4 in Radix4 and N/8 in Radix8 respectively.

![Figure 2: Radix4 Butterfly Diagram](image2)
III. FLOATING POINT OPERATION

Floating point number consists of exponent, mantissa and significant. IEEE 754 standards are used to represent the given input in 32 bit floating point numbers. In which single precision is carried out, thus the 32bit output can be obtained. Floating point number uses one bit for sign bit, 23 bits for mantissa and 8 bits for exponents.

The sign bit is used to indicate the nature of the number i.e, either positive or negative. If the sign bit is 0 then the number will be positive otherwise it will be negative.

IV. EXISTING SYSTEM

Fused dot product allows the difference of the product too along with addition that is useful in the implementation of complex multiplication. Fused floating point operation is the fused add-subtract operation. Computing the sum and difference of two floating point operands is used many times in DSP algorithms. Fused add-subtract unit performs the addition and subtraction on same pair of floating point operands in parallel fashion.
In the existing system, the Fused Dot Product Add unit is implemented in the basic FFT Radix2 architecture. Floating point operation was also included in the Radix architecture in which the latency is reduced to some extent.

V. PROPOSED SYSTEM

FDPA unit in Rdix4

Radix4 is an efficient FFT architecture, in which the number of adders and multipliers required are reduced. Four inputs and four outputs are available.

Figure 10 Timing constraints in Radix8 with FDPA

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REFERENCES