Effective Signal Capturing Using FPGA

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***Abstract*— Digital signal capture is a prime requirement in the Embedded System field. In this paper, an embedded system is built using FPGA technology having a computer interface is presented which captures any digital signals from any system effectively at very high speed and sample rate. It can be used in testing and debugging of any embedded system or equipment. This design will be developed on the FPGA platform as it will give lots of flexibility and usability in future also.**

***Keywords* -- Embedded System, Debug, FPGA, Interface, Sample Rate**

I. INTRODUCTION

In this day embedded system is a growing field in the world. In any embedded system, most of digital devices are used. These devices take some digital inputs, processes on it and give digital output. To test and debug embedded system, various equipments are used. One of the frequently used equipment is Logic Analyzer. Here in this paper, some of the additional features are proposed. In this proposed idea, Logic Analyzer will not only take the signal to be tested but also give some particular output. Before this, we need an effective technique to capture the digital signals so that system can better process on it. Various methods available to capture the signals as well as the better technique for signal capturing using FPGA (Field Programmable Gate Array) is also explained in this paper.

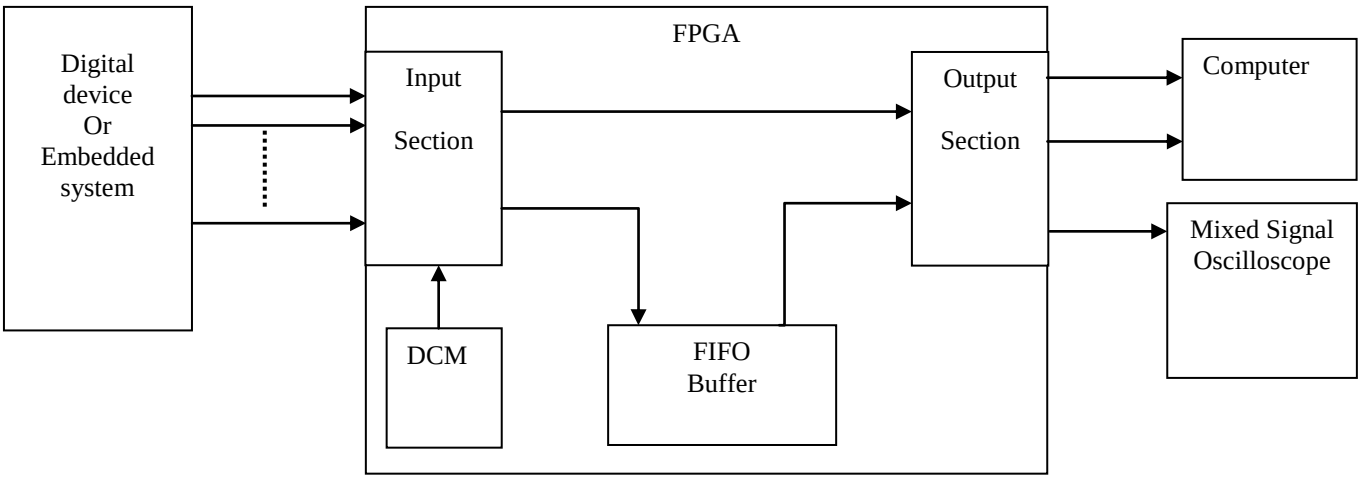

Figure 1 Simplified Block Diagram

METHODS FOR SIGNAL CAPTURE

A. *Direct feed:*

This is very simple n direct way to capture a digital signal into any device. In this technique, the connecting wire is directly connected to the device pin. In this technique it is taken care that the device must support the signal level range that the incoming signal is having, i.e. TTL, LVCMOS, etc.

B. *Analog to Digital Conversion:*

This is widely used technique. In this, the signal is given to input of A/D converter and input signal is being sampled at a fix sampling frequency. The output of the A/D converter is given to the target device. Here in this paper, another technique is proposed is explained below.

FPGA used is from the XILLINX SPARTAN 3 family. Specifically, the chip used from this family is XA3S400 which has 4pqg208 package. This chip can capture the digital signal in the range of TTL, LVCMOS and Differential signals.

II. IMPLEMENTATION

In FPGA, we can build any digital block according to our requirement. So, here also a high frequency clock is to be generated using DCM (Digital Clock Module) and PLL (phase locked loop). With the use of this high frequency clock, the input signal is captured at high sample rate. Fig. 1 shows simplified block diagram.

III. CIRCUIT OPERATION

Any random digital signal is generated from a microcontroller and it is given to any of the FPGA I/O pin. This input signal is sampled at the high sample rate at the high frequency clock signal. Here the input signal is sampled at dual edge of clock signal. It means that the input signal voltage value at the I/O pin of FPGA is checked at rising edge as well as falling edge of the clock signal.

On the other hand, these captured samples are transferred to other I/O pin of FPGA. From there, it is shown on the display. In other way, also we can transfer to any of the digital device or also we can transfer to the computer for better signal analysis using any simulator or any other software.

IV. Results and Discussion

The random digital signal generated from a microcontroller is applied to FPGA I/O pin and the output is checked with a mixed signal oscilloscope as shown in Fig. 2 below.

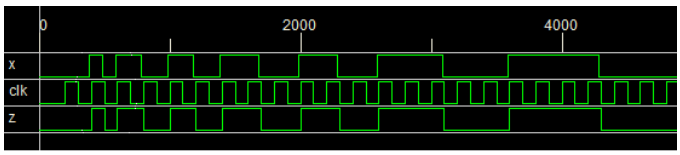

Figure 2 Signal obtained in Mixed Signal Oscilloscope

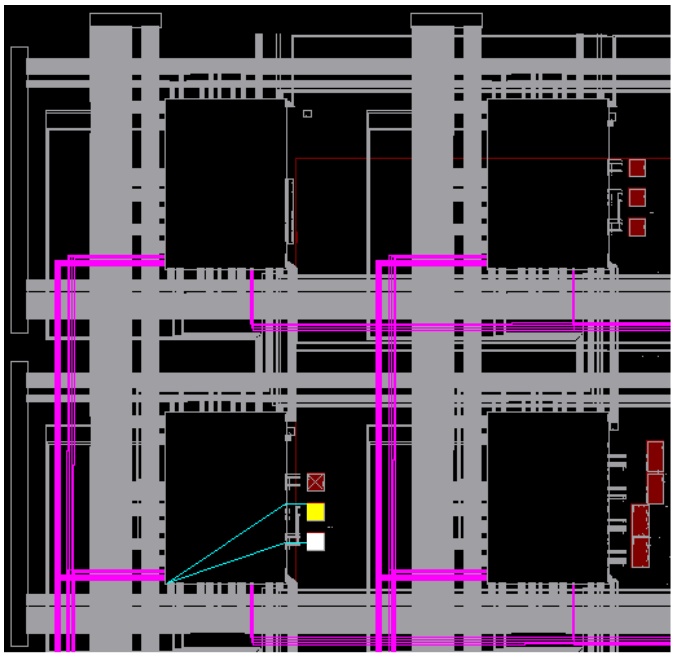

Figure 3 Routed Design

Figure 3 shows the physically routed design for the signal capturing process. This design is generated using Xillinx FPGA Editor Tool. The pin shadowed by yellow color indicates the connection for the input pin and the white shadowed pin indicates the pin connection from where the output is taken. The other portion shows the routing area and the routing tracks available in the FPGA chip. The blocks available at the periphery are the connection for the power and the ground rails to bias each module in a row and columns.

With the above shown responses and outcomes, we can say that compare to other techniques explained earlier, this technique is more suitable and also needs less number of objects. With this, we also gets the idea that this technique needs very less power as we need to provide the supply to only an FPGA chip. With the use of FPGA chip, we can also get very high speed.

V. Application

I have used this technique in my project in which I am designing a Logic Analyzer having the additional features of a Simulator. In this solution we can check any digital device's performance with any other circuit even though if we do not have that particular device.

This technique for the signal capture can be also used in wide field of electronics, computation, and automation. At the circuit design level this can be easily and effectively implemented. Wherever the speed is the important criteria with less space and less power, this idea can be implemented.

VI. Conclusion

The digital signal is captured using FPGA perfectly. Also in addition to this, various signals can be captured at various high speed signals according to user's criteria. User can also implement additional modules easily for better performance.

Acknowledgement

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