Design of low voltage low power high gain full swing operational amplifier

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***Abstract*— In this paper a design of conventional two stage CMOS operational amplifier was designed with all the transistors operated in sub threshold region, which allows low supply voltages with low power dissipation. When the transistors are operating in sub threshold region then there is an advantage of low power and low input bias current but there exist a problem in gain and full swing of the op-amp, the present approach overcomes this and maintains good tradeoff between gain, power consumption, and UGF with output swing $\pm V_{dc}$. The proposed operational amplifier operates at ±450mv power supply with 1µAmp input bias current and the design is carried out in 180nM CMOS cadence analog virtuoso spectre simulator.**

***IndexTerms*—CMOS OP-Amp, Full swing high gain Op-Amp, Operational-Amplifier, Sub threshold, 180nM.**

I. INTRODUCTION

Recent trends in analog design the designer look forward towards low power, a reduced supply voltage is necessary to decrease power consumption so this would reduce battery size and enable longer battery life time, low-power circuits are also expected to reduce thermal dissipation. To achieve the low power decreasing the supply voltage is one method, but there exist problems with transistors such as difficult operate them in saturation region. Another concern that draws from supply voltage scaling is the threshold of the transistor. A decrease in supply voltage without a similar decrease in threshold voltage leads to biasing issues [2]. Maintaining all the transistors in sub threshold region with achieving desired specifications is a challenging task to the designer. The unique behavior of the MOS transistors when they are in sub threshold region not only allows a designer to work at low input bias current but also at low voltage [2]. In order to achieve good tradeoff between supply voltage, power consumption, gain and UGF the conventional two stage CMOS operational amplifier with NMOS differential pair is considered and also to maintain good degree of stability Millar compensation is used.

This paper is organized as follows. Section 2 describes the block diagram and design of two stage CMOS operational amplifier. Section 3 presents the simulation results of proposed op-amp. Section 4 gives the comparative analysis with the previously published results. And finally Section 5 gives my conclusion.

II. BLOCK DIAGRAM OF OPERATIONAL AMPLIFIER

The conventional operational amplifier consists of mainly five stages they are Differential transconductance stage, Bias circuitry, High gain stage, Compensation circuitry, Output buffer they are cascaded as shown in Figure 1.

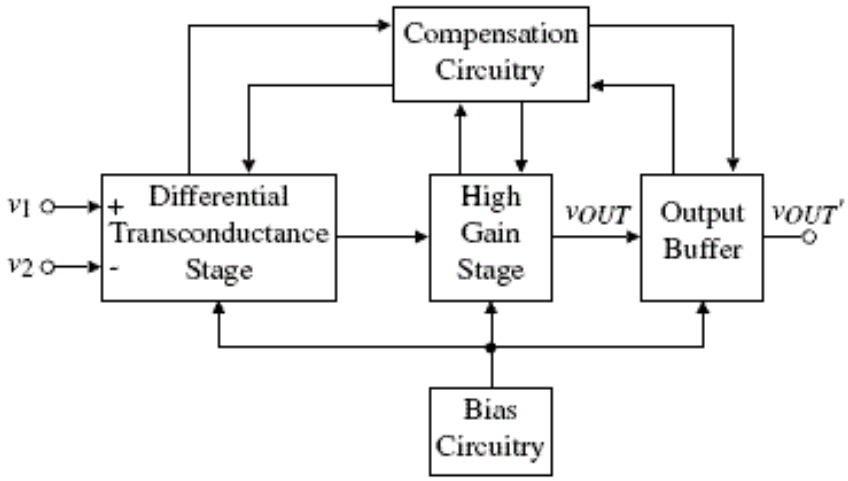


Fig.1: Block diagram of two stage CMOS Op-Amp

The very first stage of op-amp is differential trans conductance stage which converts the differential voltage to differential currents, and then they are applied to the current load hence recovering the differential voltage, the next stage consists of common source amplifier which converts the second stage voltage to the current, and finally the common source amplifier is loaded with the current sink load which converts the current into voltage at the output [3].

The transistor level schematic of the considered topology is shown in Figure 2. In that M1, M2 are the NMOS differential pair which is a differential trans conductance stage of the block diagram, M8 & M5 forms the current mirror and acts as a biasing circuit of the op-amp, M3 & M4 forms the current load ,the M7 transistor is configures as a common source amplifier with M6 current sink load. Cc acts as a compensation capacitor, here Millar compensation technique is used.

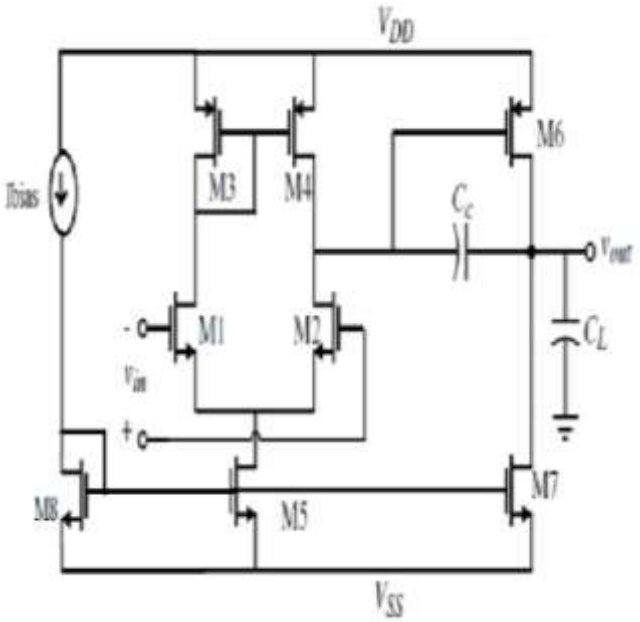


Fig.2: transistor level of two stage CMOS Op-Amp

III. SIMULATION AND RESULTS OF OP-AMP

The transistor level schematic of the proposed two stage NMOS differential pair CMOS Operational- Amplifier connected in Cadence Virtuoso ADE is shown in Figure 2.

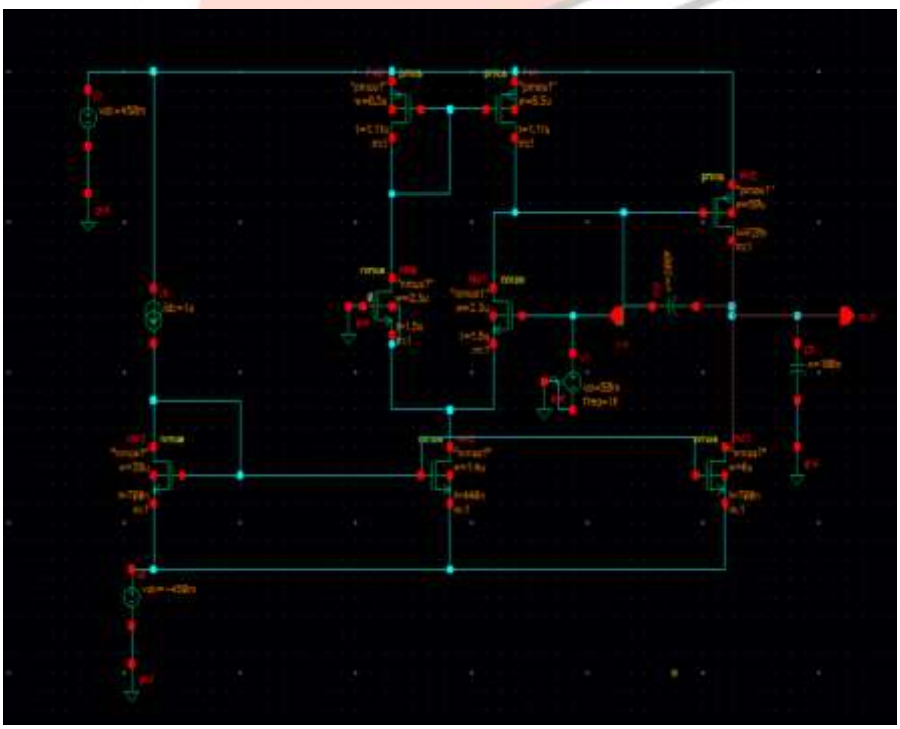


Fig.2: Schematic of proposed op-amp

In the above circuit NMOS differential pair is used at the input transconductance stage For simulation purpose the circuit is operated in single ended mode. Input specifications for the simulation in cadence are tabulated in Table 1

Table 1 Input Specifications

S.No.	Variable	Value
1	V_{dc}	±450mv
2	V_{in}	V_{sine} Freq: 1KHz. Amp: 50milli.
3	I_{bias} (Input bias current)	1µAmp.

And the transient response of the proposed circuit is shown in Figure 3.

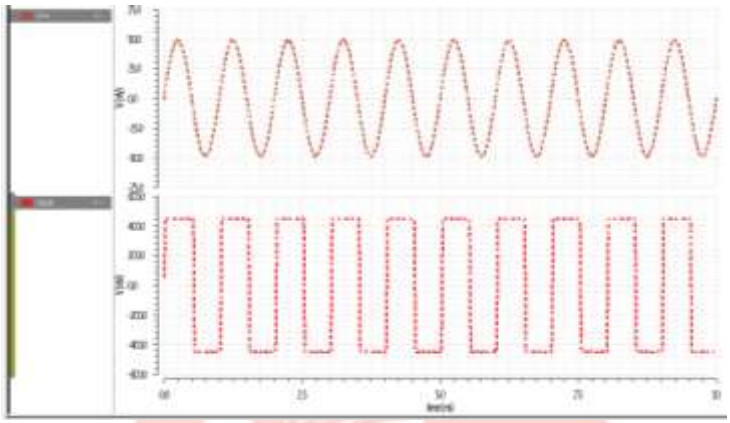
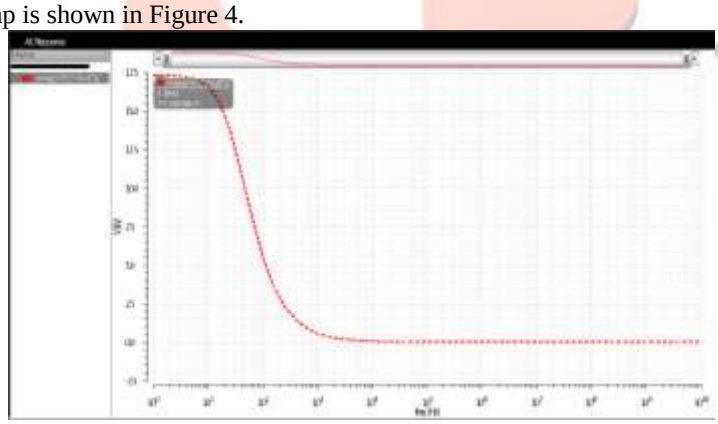
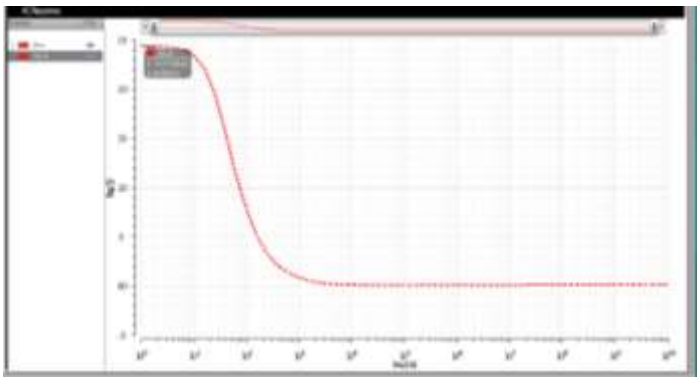


Fig.3: Transient response of the proposed circuit

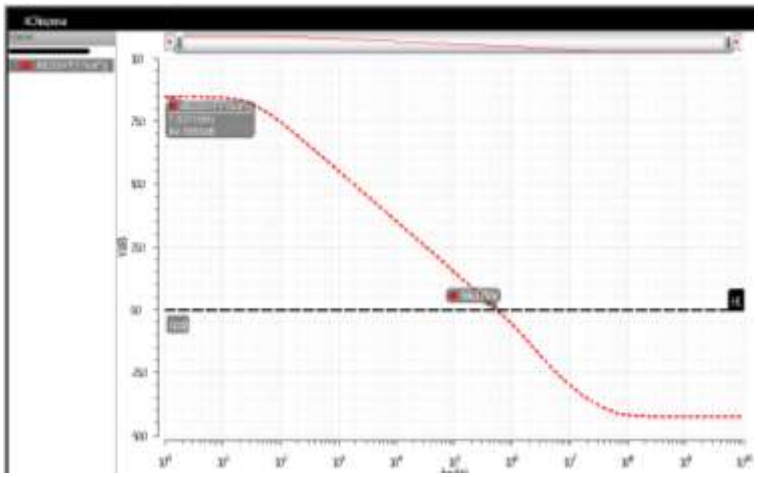
With the help of transient analysis it is clear that the circuit generates the full swing (i.e. swing between $\pm V_{dc}$). And the AC response of the proposed op-amp is shown in Figure 4.



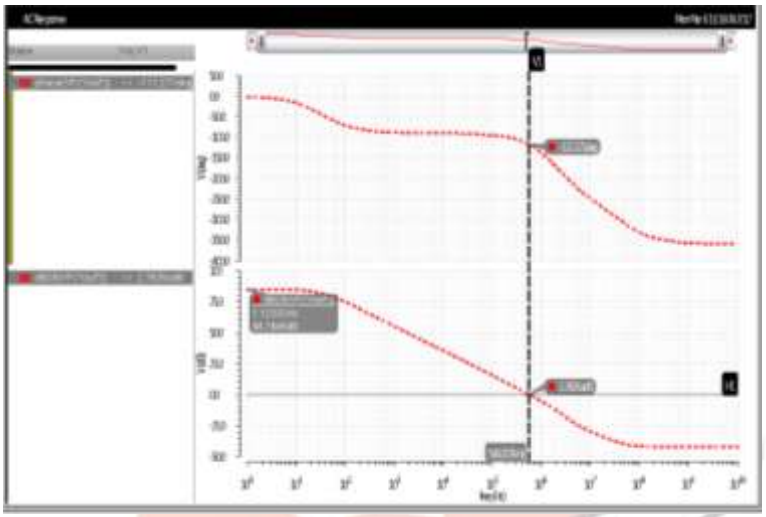
(a)



(b)



(c)



(d)

Fig.4: AC analysis of proposed circuit (a) differential mode (b) common mode (c) Gain plot (d) Phase plot

With the help of AC analysis plots the results are tabulated as

Table 2 Output Results

S.No.	Parameter	Value
1	Gain	84.76dB
2	AC magnitude (diff mode)	17.3K V.
3	AC magnitude (common mode)	2.439 V.
4	CMRR	77.016dB
5	Phase Margin	62.7 degrees
6	UGF	566.307KHz.
7	Power Consumption	523.2 n Watts

IV. SIMULATION AND RESULTS OF OP-AMP

Table 3 Result analysis

S.No.	Parameter	Paper [2]	Paper [3]	Paper[4]	This Work
1	Technology	0.8µM	180nM	180nM	180nM
2	Power supply	2 V	±1.8V	± 1.8V	450mV
3	Input bias current	1µAmp	-	-	1µAmp
4	Gain	61.11dB	70db	55.5dB	84.76dB
5	CMRR	60.3dB	-	-	77.016dB
6	Phase Margin	61 degrees	75degrees	60 degrees	62.7 degrees
7	UGF	1.09MHz	8MHz	12.6MHz	566.307KHz.
8	Power consumption	16.8µW	19.5µW	300uw	523.2nW

V. CONCLUSION

The first aspect considered in the paper was to implement the design with less than half of the nominal supply voltage and to achieve the low power consumption. We have chosen the two stage CMOS op-amp conventional circuit topology and operated all the transistors in the sub threshold region, the design is simulated by using cadence virtuoso spectre simulator with the power supply of ±450mV and achieved the gain of 84.7dB ,phase margin 62.7degrees with the total power consumption of 523nW. And the future scope of this work is to improve the UGF in trade off with the power consumption.

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