RLC Parameter Extraction and Step Input Response Analysis of Coupled High Speed Distributed VLSI Interconnects

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Abstract-In this paper,mathematicalformula are suggested to determine inductance and capacitance values and analysis of step input response of RLC coupled high speed distributed interconnects assuming the length of the line as finite and semi finite lines as well. The values of distributed resistance, capacitance, and inductance are calculated at different technology node 32nm, 45nm, 65nm, 90nm, 130nm, and 180nm. .In addition, the effect of technology and design parameters on the resistance, capacitance, and inductance of the distributed interconnects.

Index Terms-Transmission line, Semi-infinite line, Finite line, Time domain analysis, Technology node

I. INTRODUCTION

Due to scaling down in process technologies into DSM crosstalk and its effects is a major issue in On-chip high speed VLSI interconnects, therefore, crosstalk and its effects are a serious issue in the system performance. Two crosstalk fault effects, mainly, glitch and crosstalk induced delay, The crosstalk-induced delay is found to be superposition of the induced glitch and the applied signal at the victim line, and this effect is more important in affecting the circuit performance. With the scaling of semiconductor, technologies delay time of high speed interconnects are becoming comparable with clock cycles. In other word, it is possible for the voltage through an interconnect caused by a near end transition, not to completely settle before the next transition begins. The remaining voltage through line considered as an initial condition in the computation of transient response caused by the next transition. With aggressive technology scaling, the local interconnect has become more resistive, and capacitive. The global interconnect has become more inductive. As per ITRS (2011) global wire delay increases and gate delay decreases with scaling [3].

According to the most widely used analytical delay model proposed by Sotiriadis et al. [2] and [3], the delay of the ith wire ($\in \{1, 2, \dots \dots, n\}$) of an n-bit bus is given by:

$$T_i = \begin{cases} \tau_0[(1+\lambda)\nabla^2{}_1 - \lambda\nabla_1\nabla_2], & i = 1 \\ \tau_0[(1+2\lambda)\nabla^2{}_i - \lambda\nabla_i(\nabla_{i-1} + (\nabla_{i+1}], & i \neq 1, n \\ \tau_0[(1+\lambda)\nabla^2{}_n - \lambda\nabla_n\nabla_{n-1}], & i = n \end{cases}$$

Where λ is the ratio of the coupling capacitance between adjacent wires and the ground capacitance of each wire, τ_0 is the intrinsic delay of a transition on a single wire, and ∇_i is 1 for 0→1 transition, -1 for 1→ 0 transition, or 0 for no transition on ith wire.

In on-chip VLSI interconnects, modeled in RC lines these lines when modeled in RC and various parameters are investigated like crosstalk, crosstalk induced delay. However, due to increase in frequency beyond 1GHz inductive effects come into picture and become significant in current deep submicrometer technology. The inductive effect highly depends upon the switching conditions of victim with respect to its nearest neighbor's aggressor lines. In RC modeled interconnects crosstalk is maximum when the lines are switch in the opposite direction, while in RLC modeled interconnects crosstalk is maximum when lines are switch in same direction. When the frequency is increased in advancement of technology, there is decrease in signal rise/fall times. The variation of signal rise/fall time depends upon different switching patterns of interconnects. In this paper, author suggested the mathematical expression relevant to step input response of RLC modeled interconnects. The values of resistance, capacitance, and inductance calculated at different technology nodes like 180nm, 130nm, 90nm, 65nm, 45nm, and 32nm [1].

Fig. 1 illustrates the schematic views of 5-wire Bus in which central wire act as victim line and in adjacent to line two lines are aggressor line above and below to this line respectively.

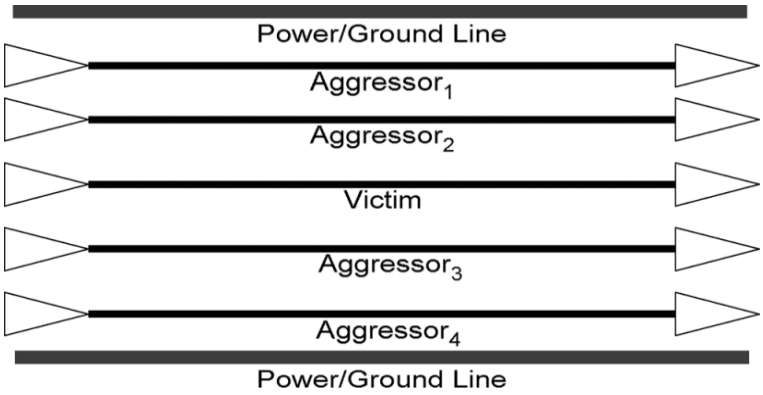

Fig. 1 Physical view of wiring of 5-bus network [1].

Three wire RLC modeled interconnect network with both coupling capacitance and mutual inductance shown below in Fig. 2

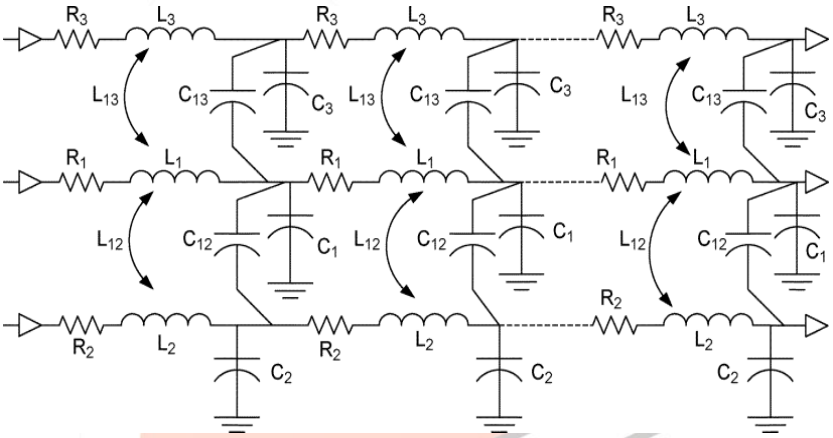

Fig. 2 3-Bus RLC Interconnect model with coupling capacitances and mutual inductances [1].

II. RLC PARAMETERS EXTRACTION

The circuit parameters are extracted using the IBM Electromagnetic Field Solver Suite Tools (EIP) [17] for the 32nm, 45nm, 65nm, 90nm, 130nm, and 180nm technology nodes [18-21] for the interconnect parameters tabulated in table 1. The operating frequency is 1 GHz with 100ps rise and fall transition times. The supply voltage is 1.8, 1.5, 1.2, 1, 0.95, and 0.9 V for the 180nm, 130nm, 90nm, 65nm,45nm, and 32nm technology nodes, respectively.

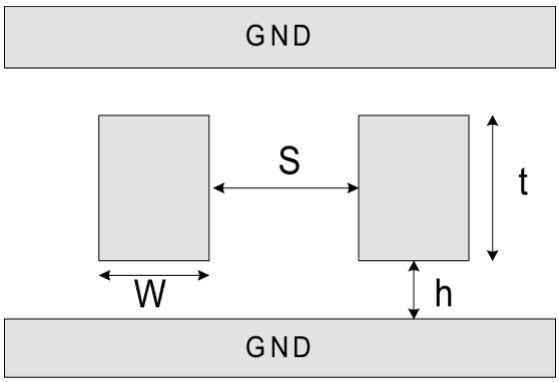

Fig .3 On-chip interconnect structure and physical dimension [2]

The interconnect line resistance is $R = \frac{\rho L}{WT}$ where ρ, L, W, and T are the resistivity, length, width, and thickness of the interconnect respectively.

The line to substrate capacitance (area and fringe flux to the underlying plane) is calculated as:

$$\frac{C_s}{\epsilon_{ox}} = \frac{W}{H} + 2.2217\left(\frac{s}{s+0.7h}\right)^{3.193} + 1.171\left(\frac{s}{s+1.51h}\right)^{0.7642}\left(\frac{t}{t+4.532h}\right)^{0.1204}$$

Similarly, the line to coupling capacitance is calculated as:

$$\frac{C_c}{\epsilon_{ox}} = 1.144\frac{t}{s}\left(\frac{h}{h+2.059s}\right)^{0.0944} + 0.7428\left(\frac{w}{w+1.592s}\right)^{1.144} + 1.158\left(\frac{w}{w+1.874s}\right)^{0.1612}\left(\frac{h}{h+0.9801s}\right)^{1.179}$$

Total capacitance of wire is calculated as:

$$C_T = C_s + 2C_c$$

Whereϵ_{ox}, h, and s are the oxide permittivity, distance, from interconnect to the substrate, and spacing between adjacent interconnects, respectively.

Now, the closed form expressions for the self and mutual inductance of a line , respectively are;

$$L_s = \frac{\mu_o}{2\pi}L\left[ln\left(\frac{2L}{w+t}\right) + \frac{1}{2} + \frac{0.22(w+t)}{L}\right]$$

and

$$L_m = \frac{\mu_o}{2\pi}L\left[ln\left(\frac{2L}{d}\right)^{-1} + \frac{d}{L}\right]$$

Whereμ_o, d are magnetic permeability of free space and the center-to-center distance between two adjacent interconnects.

Table 1
Interconnect Parameters for 32nm, 45nm, 65nm, 90nm, 130nm, and 180nm technology nodes.

Interconnect Physical Parameters	Technology nodes					
	32nm	**45nm**	**65nm**	**90nm**	**130nm**	**180nm**
Width (µm)	0.3	0.40	0.45	0.5	0.6	0.8
Spacing (µm)	0.3	0.40	0.45	0.5	0.6	0.8
Thickness (µm)	0.504	0.72	1.2	1.2	1.20	1.25
Height (µm)	0.2	0.2	0.2	0.3	0.45	0.65
P(10^{-8})Ωm	2.2	2.2	2.2	2.2	2.2	2.2
K	1.5	2	2.2	2.8	3.2	3.5
V_{DD}	0.9	0.95	1	1.2	1.5	1.8
The operating frequency is 1GHz with 100ps rise and fall transition time.						

III. TRANSIENT RESPONSE OF FINITE DISTRIBUTED

(1) STEP INPUT RESPOSNSE TO FINITE DISTRIBUTED RLC MODELED INTERCONNECT LINE [2].

The step input response of a single finite distributed interconnect at any arbitrary point through the line driven by a step input voltage shown in fig. 4 is determined as follows

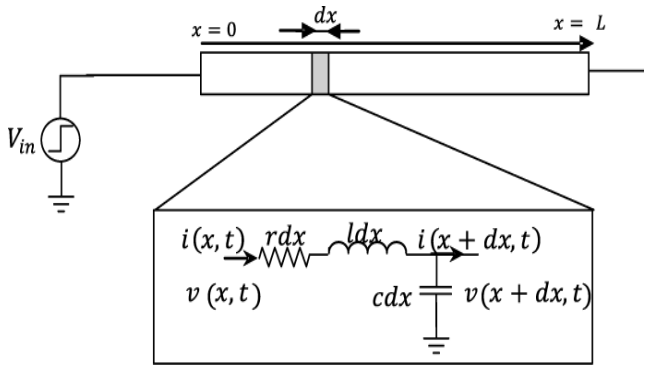

Fig. 4 Distributed RLC interconnect of length L driven by a step input [2].

The 1-D linear partial differential equation (PDE) for the next lossy transmission line. The distributed RLC model consists of a 1-D voltage equation:

$$\frac{\partial^2 V}{\partial X^2} = rc\frac{\partial V}{\partial t} + lc\frac{\partial^2 V}{\partial t^2}$$

Where r, c, and, l are the resistance, capacitance, and inductance per unit length, respectively. The boundary conditions for the RLC modeled interconnects are as follows:

$$V(x,0) = F(x); \qquad V(0,t) = U_0$$

$$V_X(L,t) = 0\,; \quad V_t(x,0) = \frac{1}{\sqrt{LC}}$$

Where F(x) is the initial voltage of the point x and U_0 is the high-level amplitude of the step signal. In addition, U satisfies the equation:

$$\frac{\partial^2 U}{\partial X^2} = rc\frac{\partial U}{\partial t} + lc\frac{\partial^2 U}{\partial t^2}$$

In addition, the conditions:

$$u(0,t) = 0; \qquad u_x(L,t) = 0$$

$$u(x,0) = f(x) - u_0$$

$$u_t(x,0) = \frac{1}{\sqrt{LC}}$$

As the variable voltage, there is infinite no. of solutions for u satisfying the boundary conditions as

$$u_n(x,t) = sinp_n x\ (A_n{}^* e^{m_1 t} + B_n{}^* e^{m_2 t}),$$

Where$P_n = \frac{(2n-1)\pi}{2L}$; here m_1 and m_2 are determined by

$$m_1 = \frac{-rc + \sqrt{r^2c^2 - 4lcp_n{}^2}}{2lc}$$

$$m_1 = \frac{-rc - \sqrt{r^2c^2 - 4lcp_n{}^2}}{2lc}$$

Now, the solution of the RLC distributed line voltage equation is as:

$$v_{RLC}(x,t) = u_0 + \sum_{n=1}^{\infty} \frac{2}{L(m_2 - m_1)} sinp_n x \left(\int_0^L (m_2 f(x) - m_2 u_0 - \frac{1}{\sqrt{LC}} \right) sinp_n x e^{m_1 t}$$
$$+ \left(\int_0^L (m_1 f(x) - m_1 u_0 - \frac{1}{\sqrt{LC}} \right) sinp_n x e^{m_2 t}$$

(2) STEP INPUT RESPONSE TO DISTRIBUTED SEMI INFINITE RLC INTERCONNECT[2]:

The voltage signal through the semi-infinite interconnects satisfies the following expression:

$$\frac{\partial^2 v}{\partial x^2} = rc\frac{\partial v}{\partial t} + lc\frac{\partial^2 v}{\partial t^2}$$

The initial conditions are:

$$v(0,t) = U_0\,; \qquad v(x,0) = f(x); \qquad and v_t(x,0) = \frac{1}{\sqrt{lc}}$$

Using AMN simplification method, one find $w = U_0$ and

$$U(x,t) = \int_0^\infty sinpx[A(p)e^{m_1 t} + B(p)e^{m_2 t}]\,dp$$

Where A(p) and B(p) are

$$A(p) = \frac{2}{\pi(m_1 - m_2)}\left(\frac{1}{\sqrt{lc}}N(p) - m_2 M(p)\right)$$

$$B(p) = \frac{2}{\pi(m_1 - m_2)}\left(m_1 M(p) - \frac{1}{\sqrt{lc}}N(p)\right)$$

Where $N(p) = \int_0^\infty sinpvdv\ and M(p) = \int_0^\infty [f(v) - U_0]sinpvdv$

IV. CONCLUSION

The motive of this paper is to extract the values of resistance, capacitance, inductance, and mutual inductance at different technology nodes like 32nm, 45nm, 65nm, 90nm, 130nm, and 180nm given in table 2 corresponding to used specification given in table 1. The operating frequency is 1 GHz with 100 ps rise and fall transition times. The supply voltage is 0.9, 0.95, 1, 1.2, 1.5 and 1.8 respectively.

TABLE -2
Line parameters calculated at 32nm, 45nm, 65nm, 90nm, 130nm, and 180nm technology nodes

Interconnect Physical Parameter	Line Parameter				
	R(Ω/mm)	L(nH/mm)	C_s(fF/mm)	C_c(fF/mm)	C_T(fF/mm)
32nm	145.5	1.8	40.68	35.92	112.5
45nm	76.39	1.74	67.94	45.58	165.1
65nm	40.74	1.66	82.03	73.22	228.5
90nm	36.66	1.653	82.94	88.37	259.7
130nm	30.55	1.64	79.13	89.44	258.1
180nm	22	1.615	80.69	81.54	243.7

Following table -3 illustrates the effect of technologyand design parameters on the resistance, capacitance, and inductance of the interconnect in which upsidearrow indicates a significant change, upside down arrow indicates a minor changes, and – indicates no change [8].

TABLE-3

	L ↑	W ↑	S ↑	T ↑
R	↑	↓	—	↓
C_s	↑	↑	↑	↑
C_c	↑	↑	↓	↑
L_s	↑	↓	—	↓
L_m	↑	—	↓	—

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