Low Cost Transmitter For A Repeater

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Abstract - There has been dramatically great demand for wireless technology in these few years. It has not only allowed to increase portability for voice and data communications but has also made easier in the deployment of systems in which wires are costly to install. There are two fundamental forces which largely fueled this demand: the need for information and the technology advancement. Inspite of the betterment of the ongoing integrated circuit technology, high performance transmitters generally use a number of discrete components and different integrated circuits because they use multiple device technologies. This thesis briefly describes advancements in both the architectural level and circuit level which make it possible in the construction of a single-chip CMOS transmitter while allowing high performance and the ability to be operated with multiple radio frequency standards. Single chip integration without the need for off-chip filtering has been addressed at the circuit level with the design of a mixer that eases the filtering requirements by canceling the closest harmonics created in the mixing process.

I. INTRODUCTION :

The technology has much improved the way in which people communicate and share information. Although many different technical methods have contributed to this evolvement, it can be finalized that the means of wireless communications has had a huge impact on modern communications as compared to other technologies. Initially in the early 20th century with progress to wireless Internet access and cellular telephony of this day, wireless communication has become vital in our life. Though transferring information without the use of wires has been a main goal, new methods have been developed which have highly reduced cost and size of the equipment as well as increasing the distance and users in the system. One particular advancement which had a huge effect on wireless communications is the making of integrated circuit technology.

The basic of wireless devices is the ability to transmit and receive signals without wiring process. The hardware finally is responsible for this function, the transceiver, is used in nearly all wireless devices except being devices that only receive, such as some devices that can only transmit. A transceiver contains two basic blocks namely the transmitter and the receiver. The transmitter is used to convert low frequency or baseband signal to a high frequency or radio frequency (RF) signal. This higher frequency signal is then radiated through the antenna. The receiver is used to convert the RF signal to a baseband signal. Transceiver design is important to be considered because it affects many faces of the device including performance, size, cost and power consumption.

A wide variety of signal processing is needed in a typical transceiver design. The necessary signal processing typically includes baseband digital, baseband analog, intermediate frequency (IF) analog, and RF analog. Commonly each of these types of processing will require an individual IC. In addition to these processing elements, the interface between the baseband analog and digital sections will typically employ a dedicated IC and a special high power analog RF chip is needed to drive the antenna. Consequently, the transceiver usually consists of many separate integrated circuits as well as large numbers of passive components. The different sections use distinct ICs because different integrated circuit technology may be best for each section. For example, the technology used for the digital portion is typically silicon CMOS but much of the analog and RF signal processing is performed by other, more expensive, technologies such as silicon bipolar, gallium arsenide (GaAs) or silicon germanium (SiGe). While this multichip solution may be advantageous for the performance of the transceiver, it also increases both the cost and size.

II. OBJECTIVES :

1. To minimize the cost of production.
2. To minimize the net power consumption.
3. To make it economical for the society.

III. SOFTWARE USED :

Cadence Design System

IV. METHODOLOGY :

An experimental investigation is to be carried out to identify the components required and to simulate followed by comparison with the current power and cost. Following are the details of experiment work

Stage I: Mixer

A critical component in both RF transmitters and receivers is the mixer. Mixers are used to frequency translate the signal either from baseband to RF, as is the case in a transmitter, or RF to baseband in a receiver. Ideally this frequency translation would occur without the generation of other, unwanted signals. This would happen if the frequency translation was implemented with an ideal

multiplier. However, in practice, multipliers are very difficult to implement and mixers are used instead. Although mixers perform the multiplication operation, they are not ideal and other unwanted signals are created in the process. The fundamental role of a mixer is to multiply two signals in the time domain. To understand why this is important for frequency translation consider two signals b(t) and c(t) defined as

$$b(t) = \cos(\omega_b t)$$

And

$$c(t) = \cos(\omega_c t)\,.$$

Based on a trigonometric identity, the multiplication of these two sinusoids results in the following output:

$$b(t)c(t) = (\cos\omega_b t)(\cos\omega_c t)$$
$$= \frac{1}{2}\cos(\omega_c - \omega_b)t + \frac{1}{2}\cos(\omega_c + \omega_b)t\,.$$

Although the input consists of two tones at frequencies ω b and ωc, after multiplication, the output consists of tones at the sum and difference of frequencies ω b and ωc.
Therefore frequency translation, both up and down, has occurred when the two signals were multiplied. Multiplication in the time domain corresponds to convolution in the frequency domain.

Stage II: Band Pass Filter

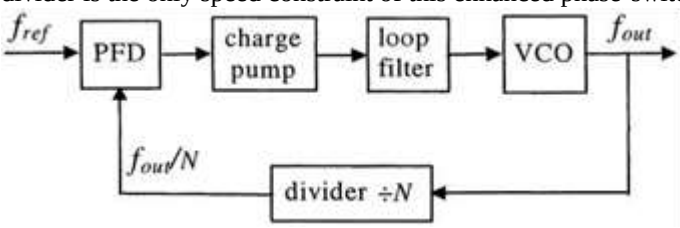
Receiver system is the important block in wireless applications. The signals present in atmosphere are easily detected and received by an antenna or antenna arrays, and fed to the next block low noise amplifier (LNA) stage for the amplification process and are filtered out some of the unwanted noise. Generally the signal received is not so strong and noisy, so band pass filters (BPF) are needed to pass only the needed signals in a bandwidth (BW) and remove noise. After passing through the LNA and BPF, the received signals are strong in strength and noise becomes less, which will be then processed by the following receiver chain that is out of the scope of this thesis.
For transmission and reception of high-quality signal, a UWB band pass filter should have the following specifications:
– Normal bandwidth of 20% or 500 MHz and greater
– A precise selectivity to reject signals from existed systems like 1.6 GHz global positioning systems (GPS), and 2.4 GHz ISM band operating systems. Recently, the UWB systems are developed and applied all over. To meet the FCC specifications, a precise selectivity at both lower and higher frequency ends and flat group-delay response over the whole band are required.

Stage III: Power Amplifier

With the development of wireless communication systems, an increasing number of communication standards have been proposed and implemented to meet the performance requirements of different applications. Since the power amplifier (PA) dominates the power consumption of the radio system, it is imperative that the PA satisfy some stringent performance requirements. Those requirements and the design target for a power amplifier include high drain efficiency, a minimum power level, linearity, multi-band and broadband operational ability, efficiency enhancement at back-off power level, etc. The major function of a power amplifier is to draw power from a direct current (DC) power supply and use the power to enlarge the input signal. Drain efficiency describes the efficiency of the transformation from DC power to radio frequency (RF) power. Since the power amplifier is the RF component that consumes most of the power in transceiver systems, the power amplifier should have high efficiency to minimize wireless infrastructure operating expenses. Also, a PA with low efficiency will result in a large amount of unused DC power heating up the transistor and consequently affecting transistor performance. To enhance the efficiency of a power amplifier, several classes of operation have been proposed to shape the output voltage and current waveform so that DC power consumption can be minimized. Since output voltage and current waveform can be affected by the termination at both fundamental and harmonic frequencies, some operation modes use harmonics to re-shape the voltage and current waveform for better PA performance. The classes of operation mode can be categorized in two types. In one type, a transistor acts as a voltage controlled current source, and output power will depend on the input signal. This kind of operation mode includes Classes A, AB, B, J, C, F/F-1, etc. In the other type, such as Class E or Class D operation mode, a transistor acts as a switch that will turn on and off depending on the input signal.

Stage IV: Local Oscillator

To provide a further insight into the switching operation in the proposed phase-switching architecture, a detailed delay timing analysis of the switching control loop is given. By calculating the delay budget in the loop, we conclude that usually the first ÷2 divider is the only speed constraint of this enhanced phase-switching architecture.



The loop filter is a barrier in fully integrating a narrow-band PLL because of its large integrating capacitor. To make the loop capacitance of a narrow-band PLL as small as possible while keeping the same loop bandwidth, designers increase the loop resistance and reduce the charge-pump current.

Stage V: Charge Pump

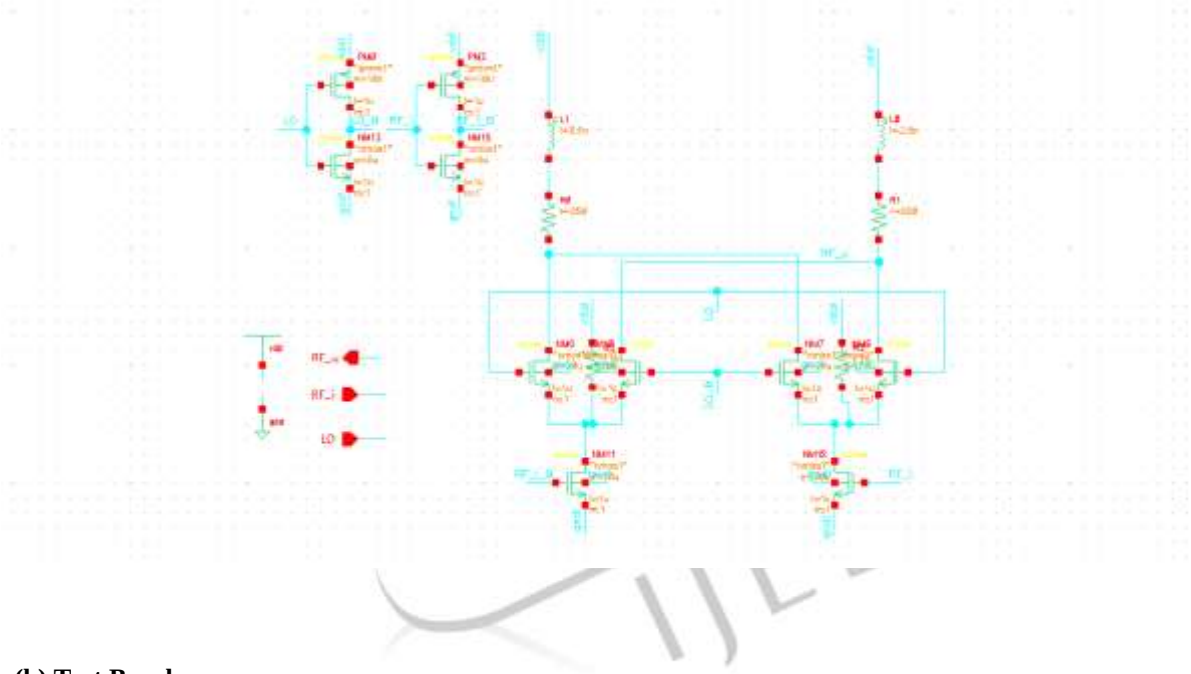
There are three types of filters, low pass, high Many systems incorporate a mixture or hybrid of these basic approaches in order to take advantage of the benefits of increased speed or improved resolution that one approach may have over another. For example, sometimes a PLL synthesizer may incorporate a DDS in its reference circuitry to increase resolution or to reduce switching time [47]. A major drawback of this approach is that the PLL acts as a multiplier on any phase noise or spurs in its reference and a DDS may have high spurs. The resulting noise at PLL output can seriously degrade system performance In a real PLL, the inaccuracy of resistance and capacitance of an on-chip loop filter and variance of VCO conversion gain affects the phase margin. The variation of resistance and capacitance is typically 10%~20%, while the variation of can be more than a factor of 2. Therefore, we have to keep enough phase-margin to accommodate variations of design parameters. Figure 3-9 illustrates the PLL phase margin for different values from 5 to 30, when deviates from its optimal value of

It shows that the phase margin is not much sensitive to the variation of and ratio. For example, in case of the optimal phase margin is 55°, and it degrades to 48.7° when ω_c deviates from its optimal value by a factor of 2, i.e., $\pm 6dB$.

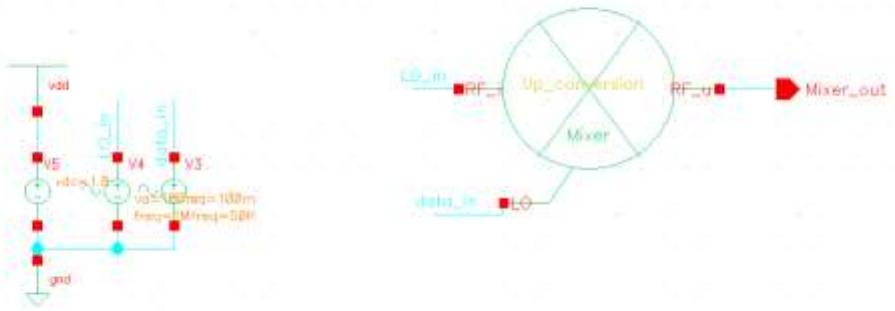
Stage VI: Results:

1. **Mixer:**

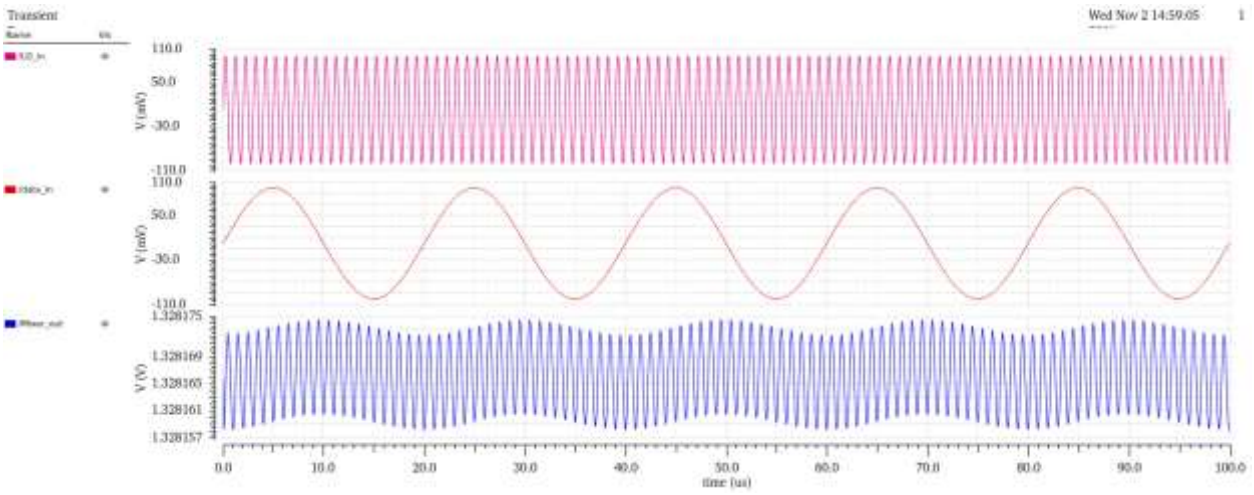
(a) Circuit Schematic:



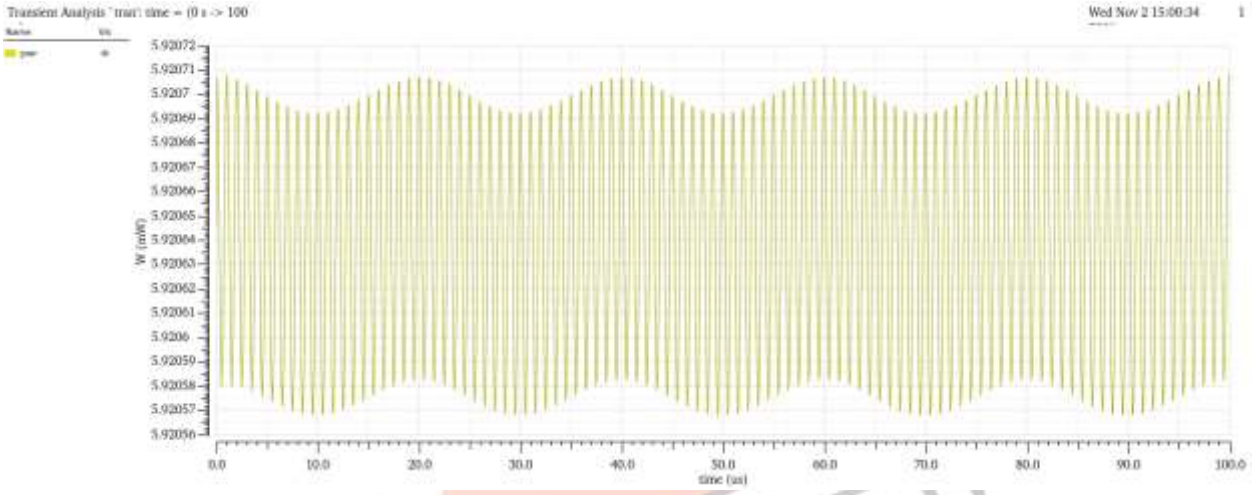
(b) Test Bench:



(c) Transient Analysis:

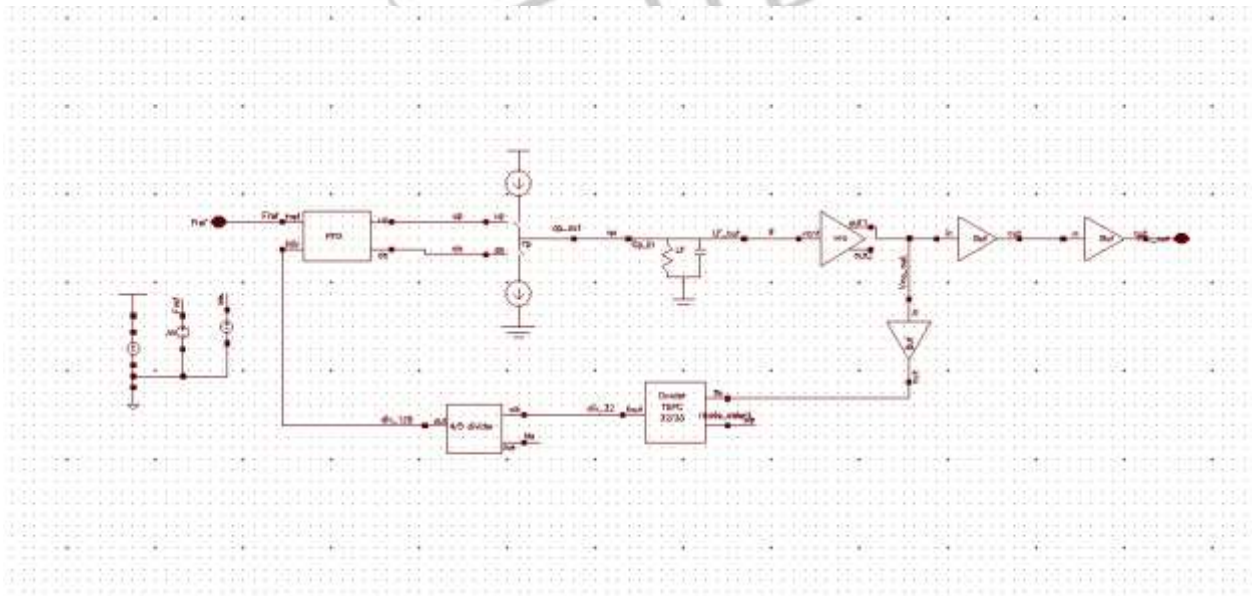


(d) Power Waveform Analysis:

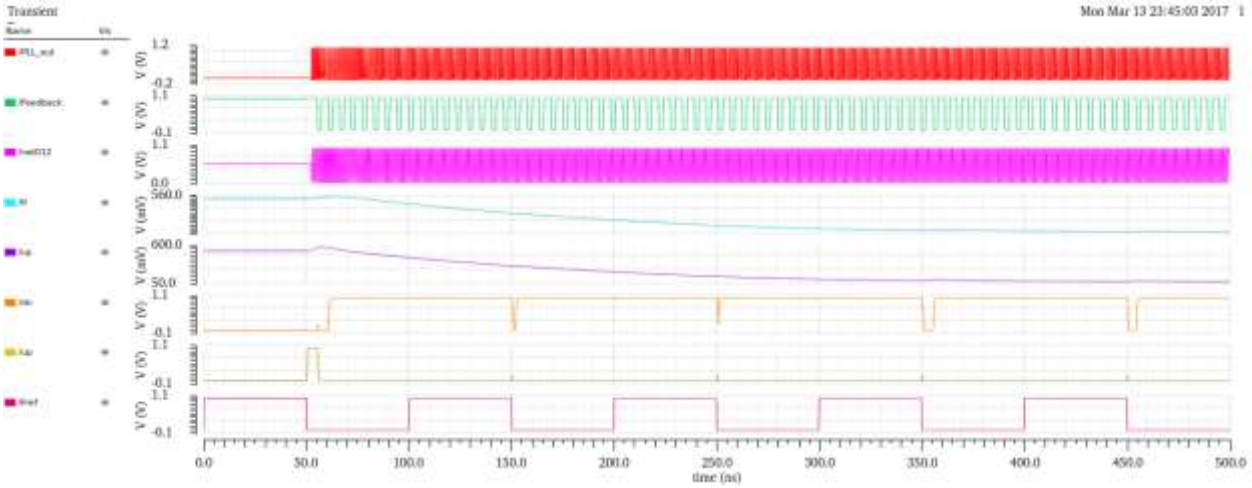


2. Local Oscillator:

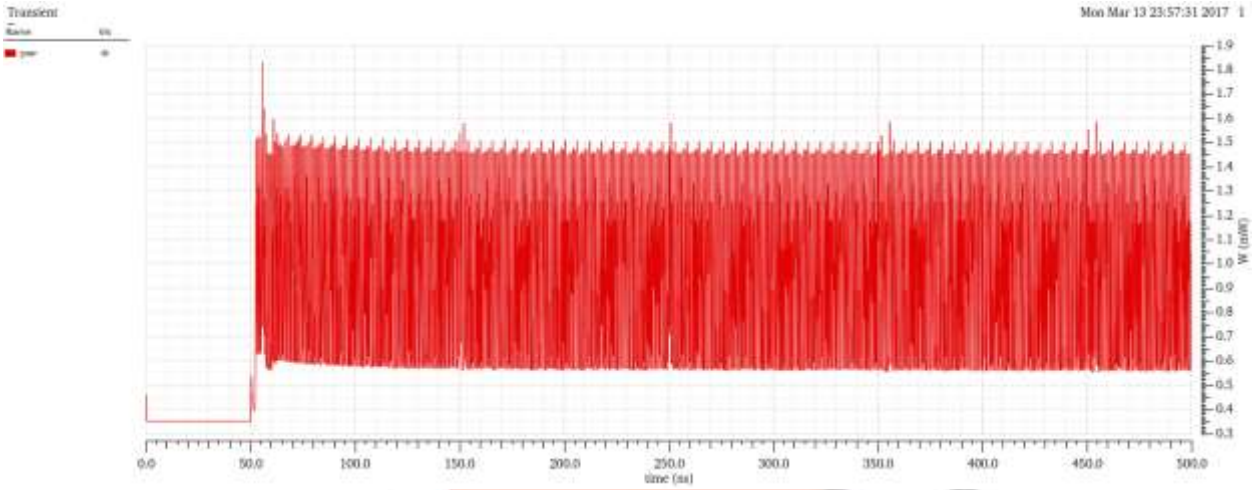
(a) Circuit Schematic:



(b) Transient Analysis:

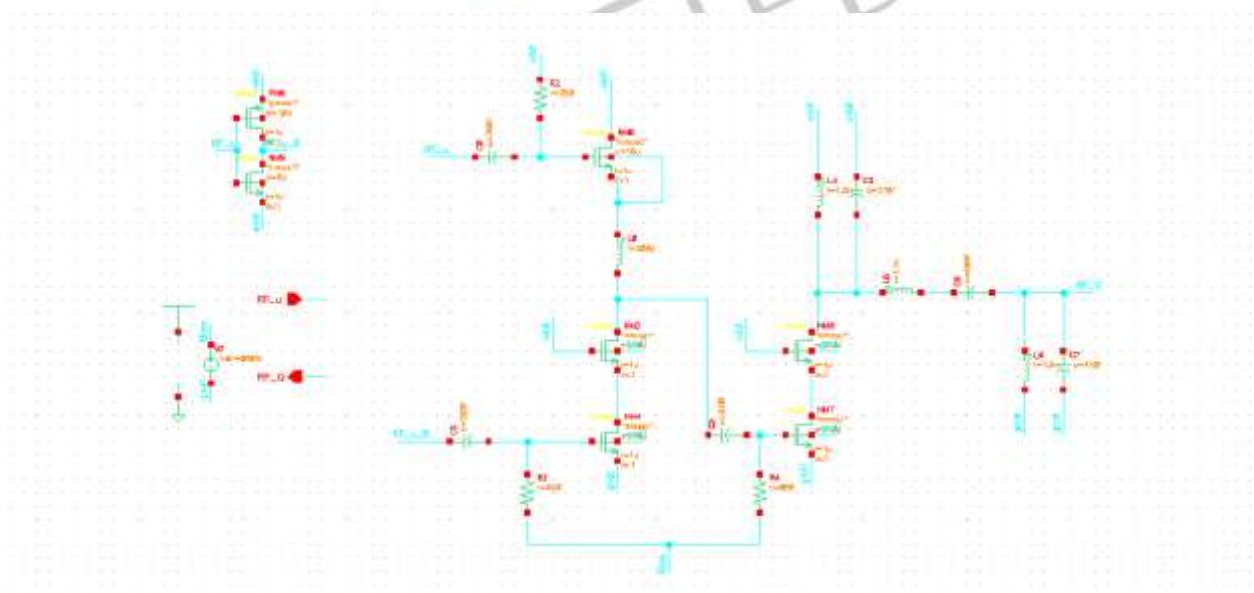


(c) Power Waveform Analysis:

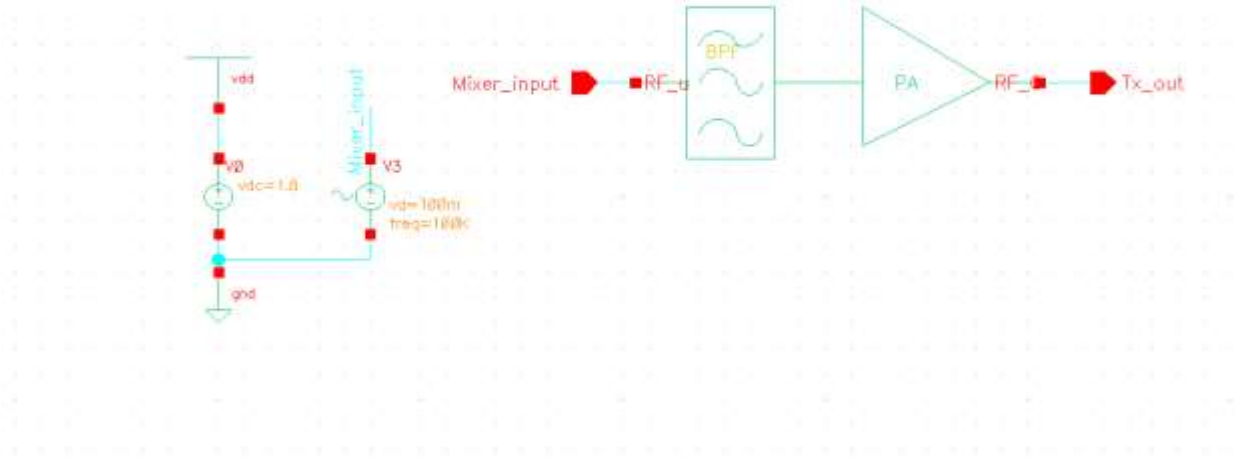


3. BPF with PA:

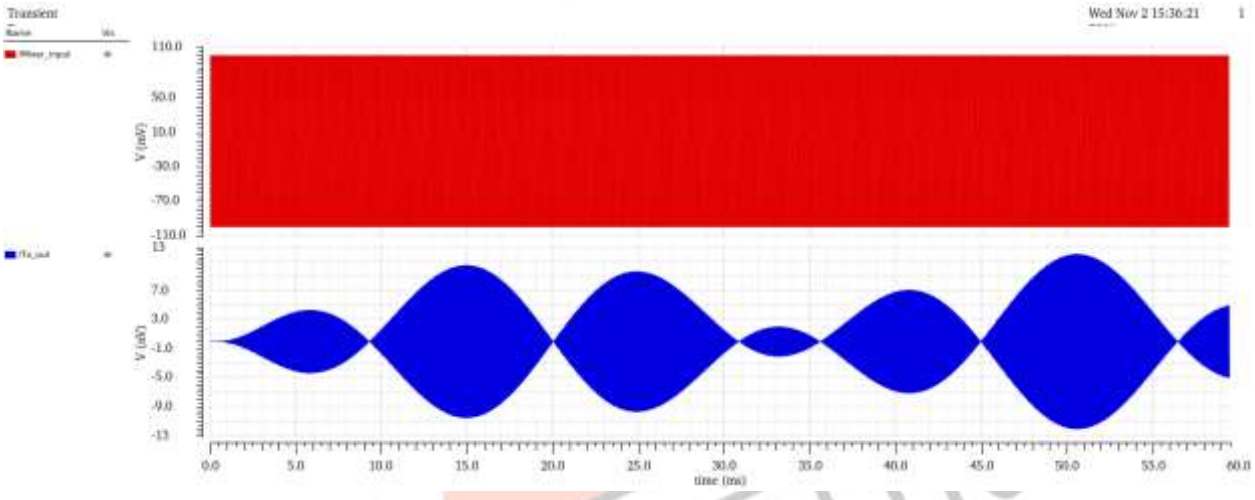
(a) Circuit Schematic:



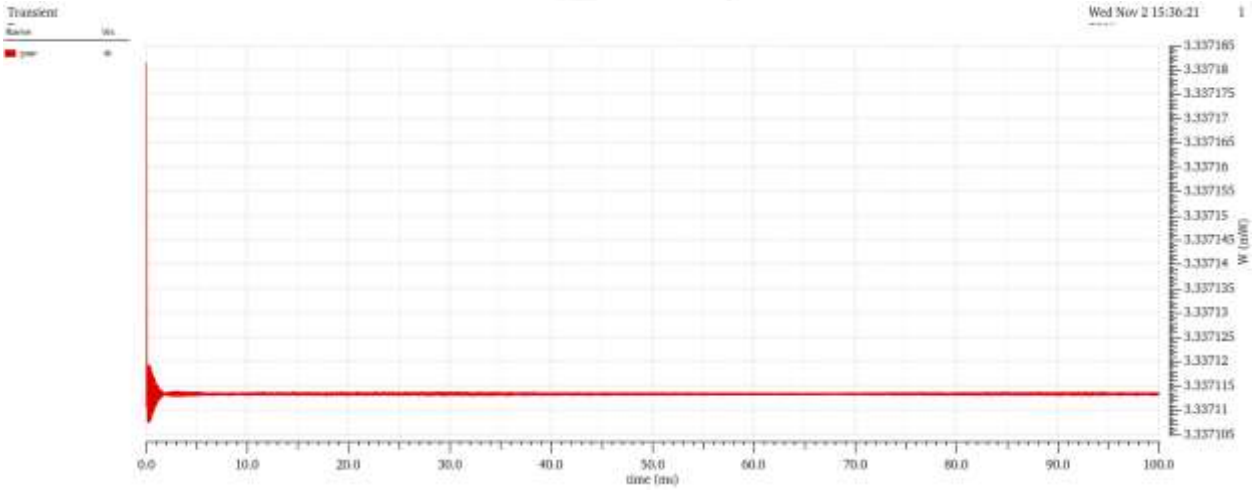
(b) Test Bench:



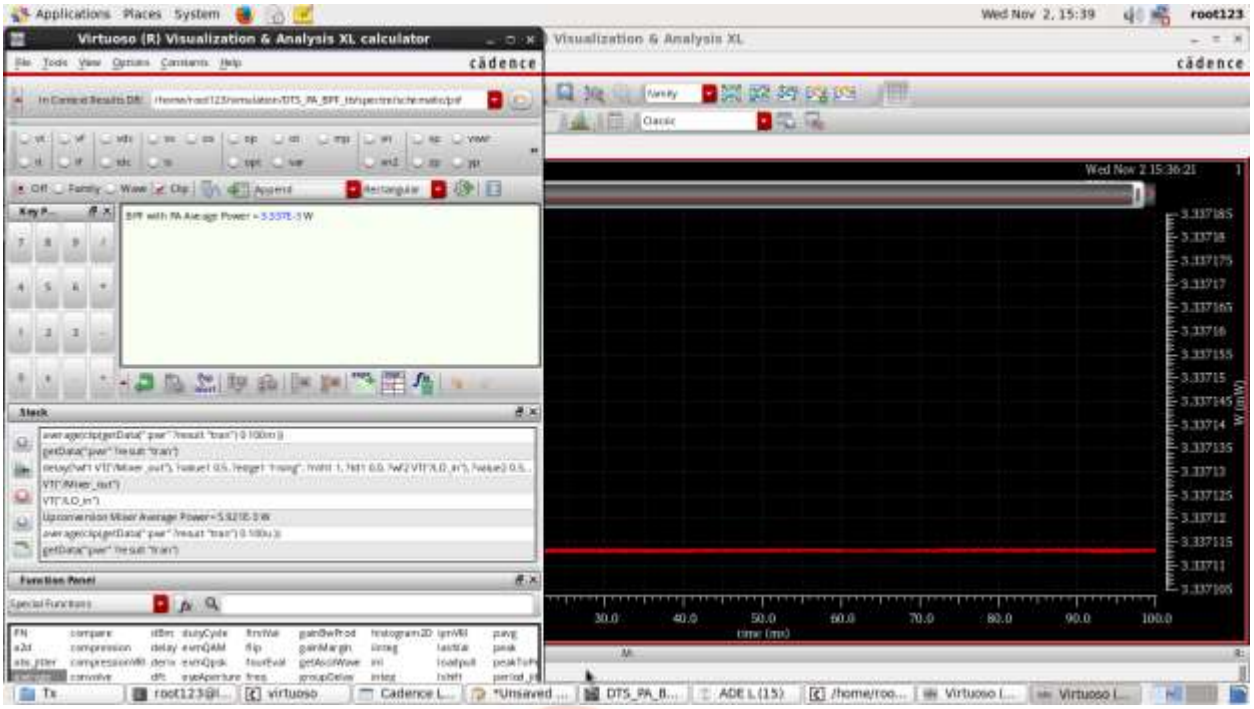
(c) Transient Analysis



(d) Power Waveform Analysis:



(e) DC Power Consume:



Discussion on Results

The simulation was performed in Cadence tool one by one and the results obtained are shown above. From the result we concluded that the net power consumed and cost of the product have been reduced widely.

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