Comparison of Conventional low Power Flip Flops with Pulse Triggered Generation using Signal Feed through technique

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***Abstract*— the objective to design and compare a low-power flip-flop (FF) design presenting an explicit type pulse-triggered framework. Pulse triggered method use used for clock to resolves lengthy discharging path issue in conventional explicit type pulse-triggered FF (P-FF) design and achieves better rate and energy efficiency. A novel power effective pulse triggered flip-flop design with lowest no. of transistors is suggested. Various publish structure simulator outcomes based on Mentor Eldo Simulator CMOS 180-nm technology.**

Index Terms— Flip flop, low power, pulse triggered, signal feed through.

I. INTRODUCTION

Flip-flops (FFs) are the fundamental storage components applied thoroughly in a myriad of digital designs. Specifically, digital designs today usually undertake intense pipelining methods and use several FF-rich moduler s like shift register ,register files and first in first out.

It can also be projected that the ability use of the clock system, which includes clock distribution network and storage components, can be as large as 50% of the full total system power. FFs hence lead a substantial part of the chip region and energy use to the entire system design.Pulse-triggered FF (P-FF), due to its single-latch framework, is very popular compared to the conventional transmisson gate (TG) and master–slave centered FFs in high-speed applications. Form rate gain, their signal ease reduces the ability use of the clock tree system.

A P-FF is made up of pulse generator for strobe signal and a latch for information storage. If the triggered pulses are effectively thin, the latch works as an edge-triggered FF. Because only 1 latch, instead of two in the conventional master–slave arrangement, is required, a P-FF is easier in circuit complexity. That results in a greater toggle rate for high-speed procedures. In this brief we present a noval low-power P-FF design based on a signal feed-through scheme. Seeing the delay difference in securing information "1" and "0," the design handles to limit the lengthier delay by feeding the input signal right to an inside node of the latch design to increase the info transition. That device is design by presenting an simple pass transistor for additional signal driving. When combined with the pulse generation circuitry, it types a brand new P-FF style with improved pace and power-delay product (PDP) performances.

P-FF design using signal feed throughPF-FFs, with regards to pulse genration, could be labeled being an implicit or an explicit type. Within an implicit form P-FF, the pulse generator is part the latch design and no explicit pulse signal are generated. Within an explicit form P-FF, the pulse generator and the latch are split up. Without generating pulse signal externally , implicit form P-FFs come in common more power-economical. Nevertheless, they have problems with a lengthier discharging route, leading to poor timecharacteristics. Specific pulse genration, on the opposite, incurs more energy use nevertheless the reason divorce from the latch design provides FF design an original rate advantage. Their energy use and the signal difficulty could be successfully decreased if one pulse generator is gives a small grouping of FFs (e.g., an n-bit register).

II. CONVENTIONAL APPROACHES

Explicit Pulse Data Close To Output(ep-DCO)

It has a NAND-logic-based pulse generator and a semidynamic true-single-phase-clock (TSPC) organized latch design. In that P-FF design, inverters I3 and I4 are accustomed to latch information, and inverters I1 and I2 are accustomed to maintain the interior node X. The pulse width is decided by the delay of three inverters. That design is suffering from a critical problem, i.e., the interior node X is cleared (discharged) on every rising edge of the clock instead of the existence of a static input "1". This provides increase to big switching energy dissipation.

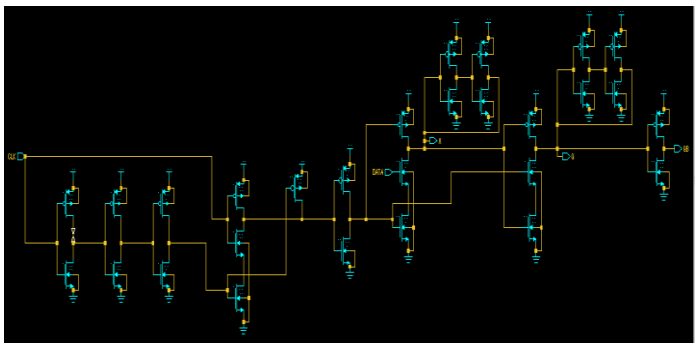

Fig.1(a) ep-DCO

Conditional Discharged Flip Flop

Fig.1(b) shows conditional discharged (CD) approach , a further n-MOS transistor MN3 managed by using the output input statistics remains " 1 ". The keeper logic for the inner node X is simplified and includes an inverter plus a pull-up pMOS transistor only.

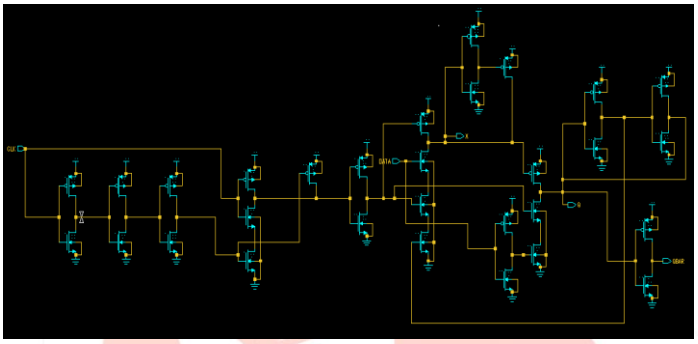

Fig.1(b) CDFF

Static Conditional Discharged Flip Flop

Fig. 1(c) shows an identical P-FF design (SCDFF) utilizing a static conditional discharge approach . It varies from the CDFF design in utilizing a static latch structure. Node X is hence exempted from periodical precharges. It displays a lengthier data-to-Q (D-to-Q) delay compared to CDFF design. Equally designal experience a worst situation delay the result of a discharging path consisting of three loaded transistors, i.e., MN1–MN3. To over come that delay for greater rate efficiency, a powerful pull-down circuitry becomes necessary, that causes additional format region and energy consumption.

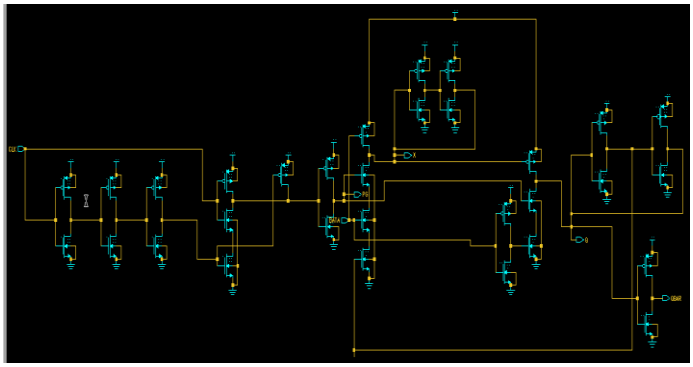

Fig.1(c)SCDFF

Modified Hybrid Latch Flip Flop

The modified hybrid latch flipflop (MHLFF) found in Fig. 1(d) also works on the static latch. The keeper logic at node X is removed. A weak pull-up transistor MP1 managed by the output indicate Q retains the level of node X when Q equals 0. The MHLFF design have two drawbacks. First, because node X isn't predischarged, a extended 0 to at least one delay is expected.

The delay drops more, must be level-degraded clock pulse (deviated by one VT) is used to the discharging transistor MN3. 2nd, node X becomes floating in certain cases.

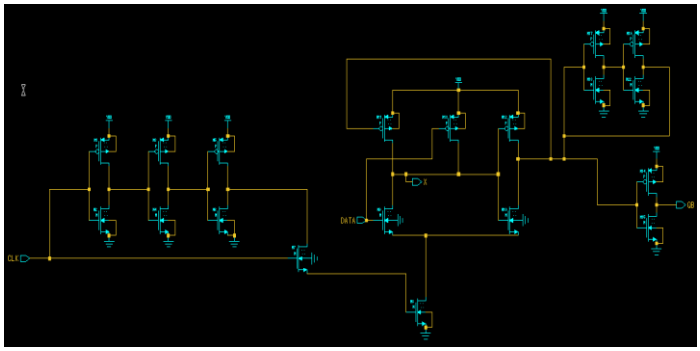

Fig.1 (d)MHLFF

Single Ended Conditional Capture Energy Recovery

Figure 1(e) shows a refine low power P-FF design called simple finished conditional record power healing(SCCER) utilizing a conditional discharged technique. In that design, the keeper logic (back-to-back inverters I7 and I8 in Fig. 1(a)) is changed by a weak pull up transistor P1 in line having an inverter I2 to reduce the load capacitance of node X. The discharge way includes nMOS transistors N2 and N1 linked in series. So as to eliminate unnecessary switching at node X , a supplementary nMOS transistor N3 is employed. Because N3 is managed by Q_fdbk, no discharge does occur if input stays high. The worst situation moment with this design does occur input knowledge is "1" and node X is discharge through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A strong pull-down circuitry is therefore required to make certain node X may be effectively discharged. That means broader N1 and N2 transistors andan extended delayt from the delay inverter I1 to broaden the discharge pulse width.

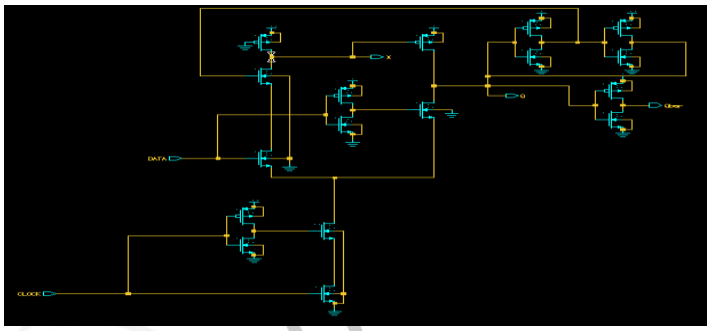

Fig.1(e)SCCER

The modified pulse triggered flip flop

The modified pulse triggered flip flop reduces the number of transistors stacked in the discharging path and also reduces the overall power consumption by which the overall efficiency of the designed circuit is improved. The modified conventional pulse triggered FF design works on rising edge of the clock pulse. When the clock is in rising edge (MN3, MNx turns ON) and the data is '0' then the transistorMN1 turn OFF, the pull up transistor MP1 turn off because the node X is charged and the data '0' pass through the pass transistor, turn the drive node Q to '0' and saved to the latch circuit.

When the data is '1' then the transistor MN1 turn ON this will turn ON the pull up transistor MP1 because node X gets the discharging path and the data '1' pass through the pass transistor, turn the drive node Q to '1' and saved to the latch circuit. In this design MN2 is connected to data its self which gives low power dissipation to the circuit.

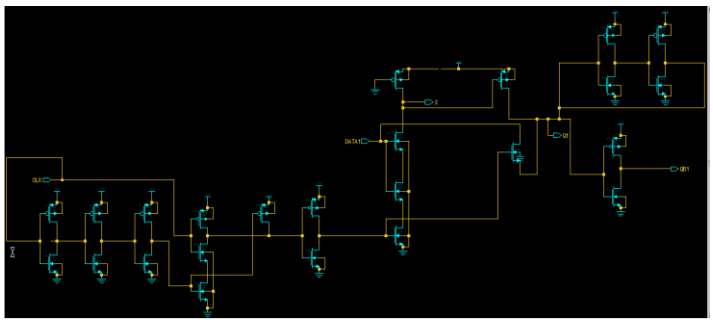

Fig 1(f) Modified pulse triggered Flip flop

III. SIMULATION RESULTS

Explicit Pulse Data Close To Output(ep-DCO)

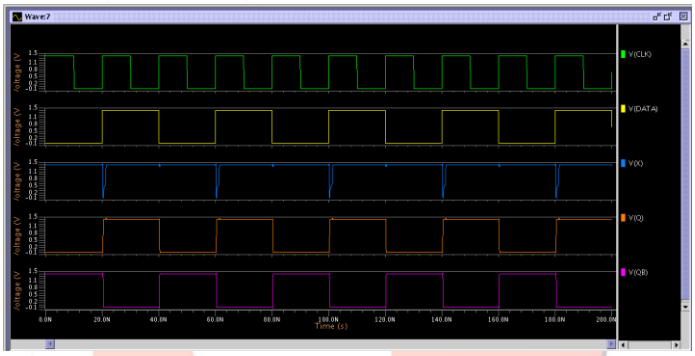

Fig 2 (a) Output waveform of ep-DCO

Conditional discharge flip flop(CDFF)

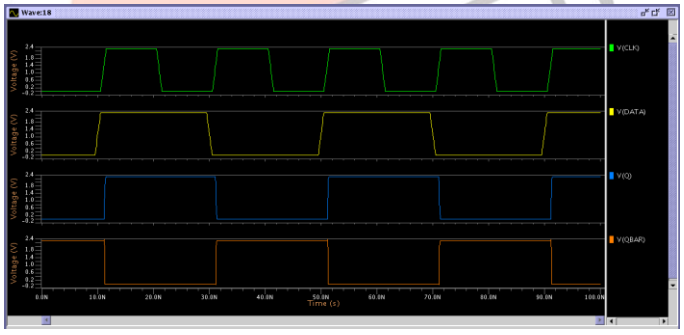

Fig 2(b) Output waveform of ep-DCO

Static conditional discharge(SCDFF)

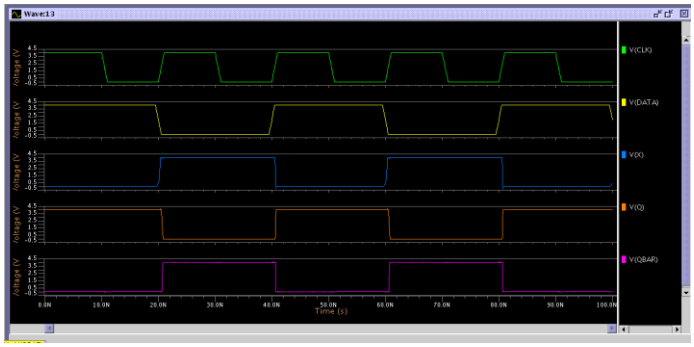

Fig 2(c) Output waveform of SCDFF

Modified Hybrid Latch Flip Flop(MHLFF)

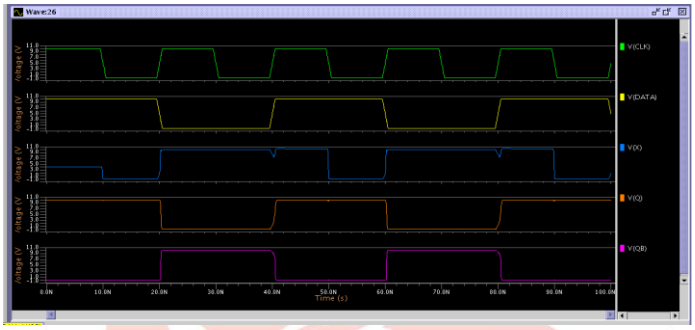

Fig 2(d) Output waveform of MHLFF

Single Ended Conditional Capture Energy Recovery (SCCR)

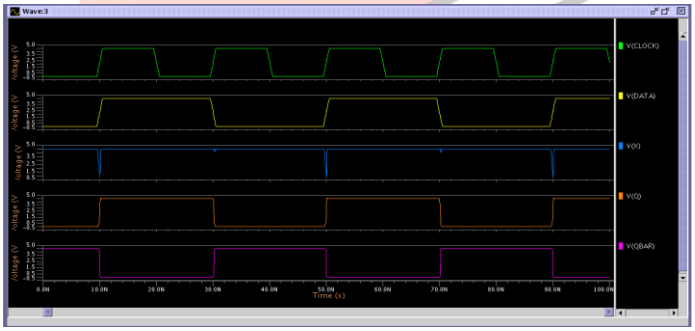

Fig 2(e) Output waveform of SCCR

The modified pulse triggered flip

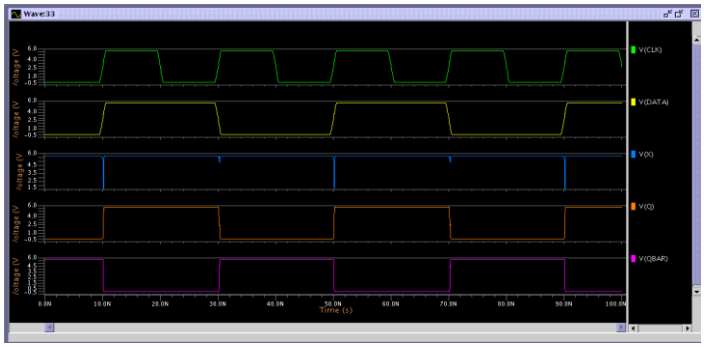

Fig.2(f) Output waveform of The modified pulse triggered flipflop

TABLE I. COMPARISION OF VARIOUS FF DESIGNS

Flip flop	**No. transistors**	**Memory Size Allocated In Mb**	**No. Nodes**	**Power dissipation**
ep-DCO	28	368.3	72	137.5598 pW
CDFF	30	368.3	78	386.3947pW
SCDFF	31	368.2	63	20.867nW
MHLFF	19	368.2	50	1.636nW
SCCR	17	368.2	46	4nW
Modified PT flip flop	24	368.2	58	1.3883nW

IV. CONCLUSION

The different conventional explicit type flip flops are analysed. The power and delay calculation of conventional pulse triggered flops are done. The proposed low power flip flop using signal feed through scheme is deigned.. Here the signal feed through from input source to the internal node of the latch has extra driving to shorten the transition time. The proposed design outperforms in terms low power and high speed. Leakage, static and dynamic power are reduced in the proposed design compared to conventional flip-flops. The power and delay calculation of the proposed design is carried out. Delay is also reduced and hence the proposed design outperforms the existing flip flop.flip

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