Unified Power Quality Conditioner for Improving Power Quality Using Ten Switch Inverter

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Abstract— **The power system arrangement of three-phase-three-wire UPQC consists of two back-to-back connected six switch inverters. For this arrangement, out of twelve switches, six of the series inverter switches will be utilized most of the time. To improve the semiconductor utilization and therefore to reduce the total switch count, this paper proposes a new reduced switch topology for UPQC. The proposed topology is accomplished using only ten switches and retains all the performance merits of the twelve-switch UPQC while minimizing its underutilization without increasing the switch VA rating. This provides a detailed analytical study and evaluation by comparing the proposed topology with the twelve and nine switches based UPQC system configurations. The feasibility of the proposed topology is validated through experimental investigation.**

Index Terms— **Unified Power Quality Conditioner (UPQC), Point of Common Coupling (PCC), Voltage Source Inverter (VSI), Total Harmonic Distortion (THD).**

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I. INTRODUCTION

The ever increasing use of solid state technology in industrial and domestic applications is extensively contributing towards line current harmonics, non- linear voltage drops, cables overheating, poor power factor and more power losses at distribution levels. To mitigate these problems and maintain the reliability of the delivered power within acceptable margins, stringent power quality standards are put into practice. The adherence to these standards can be achieved with a custom power device such as the unified power quality conditioner (UPQC). Being an adaptable and flexible power electronic device, UPQC has become the most appealing solution to power quality problems at the distribution level.

A UPQC usually consists of two voltage source inverters (VSI), connected in shunt and series arrangement with the grid, at the point of common coupling (PCC) and divide a common dc link capacitor. The series VSI protects the downstream loads from sags/swells in the PCC voltage whereas the shunt VSI reduces the upstream line losses by remunerating the harmonic distortion and reactive component of the load current. When the voltage at PCC is distorted, the series VSI can be further controlled to mitigate and prevent the voltage harmonics from reaching the load. There is an extensive literature available on UPQC and a detailed review can be found.

Even if back-to-back UPQC with twelve switches provides independent control of both VSIs and excellent mitigation of grid disturbances, its series VSI is generally underutilized. During normal conditions the series VSI (six out of twelve switches) tolerate either completely inactive or perform at very low modulation index. This under-utilization of the series VSI may give rise to calculating problems.

This task proposes a new reduced switch UPQC system topology that consists of ten switches in total. The main purpose is to decrease the overall switch count of the back-to- back UPQC system whilst retaining its operational characteristics without any performance swapping. To track the linear modulation range and uniform switching frequency for all the switches in under the proposed topology, a carrier based double zero sequence injection scheme is also evolved. An appropriate control algorithm is developed to achieve the flawless operation of the proposed UPQC topology under unusual operating conditions. An experimental study is carried out to legalize the performance of the proposed topology.

II. THREE PHASE THREE WIRE UPQC SYSTEM CONFIGURATION

For three-phase-three-wire system, usually, the back-to-back inverter based UPQC system is widely used and is shown in fig. 1. It comprises of twelve power semiconductor switches in total {SA1, SB1, SC1, SA2, SB2, SC2} constitute the shunt VSI which is connected at the PCC, whereas, the switches { SA1', SB1', SC1', SA2', SB2', SC2'} constitute the series VSI and is connected between PCC and load. Both inverters share the common dc link capacitor. As shown in fig. 1, the twelve-switch UPQC deploys two dedicated inverters for performing the UPQC functionalities.

This feature permits UPQC to have shunt VSI connected at either the PCC or load with no effect on the compensation ability. Recently, there has been an effort to reduce the total switch count of the UPQC. By merging the lower three switches of the shunt VSI { SA2, SB2, SC2 }and upper three switches of the series VSI { SA1', SB1', SC1' } in fig. 1, the reduced nine-switch UPQC topology is achieved. The configuration has a set of three shared switches { SA12, SB12, SC12 } as illustrated in fig. 2. The configuration features saving of three switches and executes adequately under normal and sag conditions without an increase in the dc link voltage. However, it causes considerable rise in the switch current ratings of two switches per phase which is mainly allocated to the series connection of three switches in each lag. Therefore, six out of nine switches must be oversized for adequate

operation of the nine-switch UPQC. In addition, all the nine switches must carry on operational irrespective of the UPQC compensation mode. Thus, the reliability of the nine-switch UPQC reduces for a single switch malfunction.
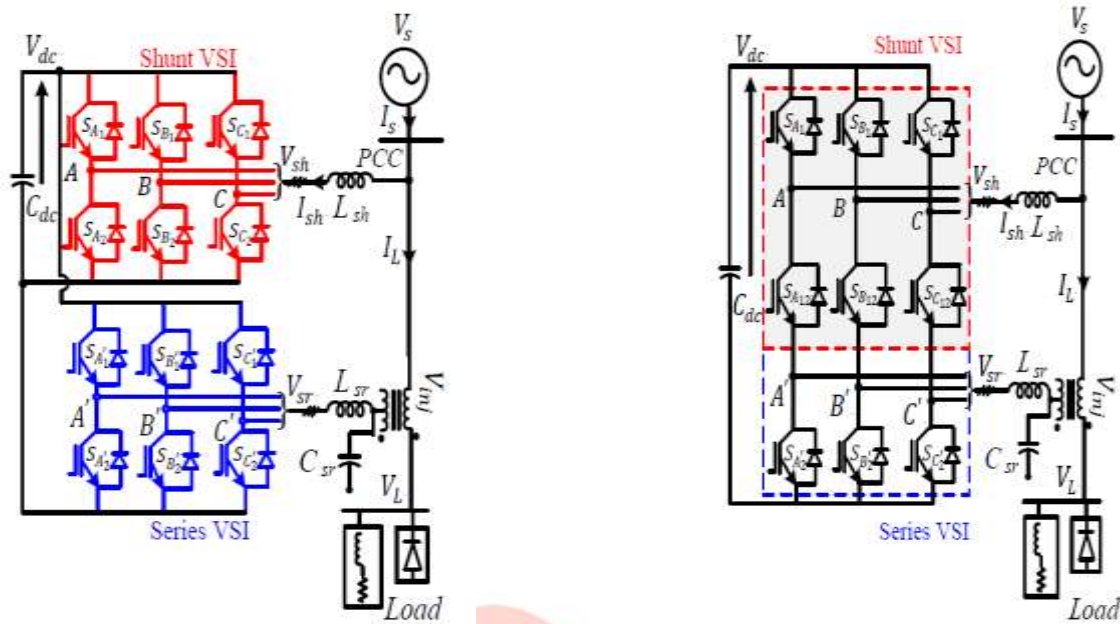

Fig. 2.1 Twelve Switch UPQC Topology and Nine Switch UPQC Topology

III. PROPOSED TEN SWITCH UPQC TOPOLOGY

A new topology of UPQC, based on ten switches, is proposed for power quality enhancement applications. As depicted in Fig. 3.1, the proposed topology is realized by combining the phase C switches of shunt and series VSI {SC1, SC2} and {SC1', SC2} in Fig. 2.1, respectively, into a common leg with a shared set of two switches SC1 and SC2. Until now the ten-switch structure has been utilized in drives applications with certain restrictions. The following subsection provides an overview of the ten-switch similar work in the literature.
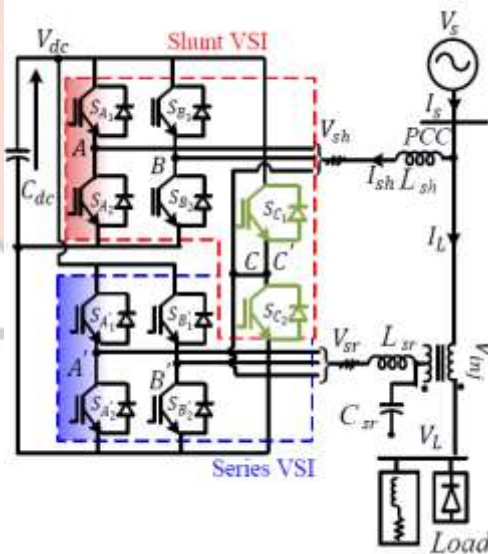

Fig. 3.1 Ten Switch UPQC Topology

Existing constraints and background work

Like most reduced semiconductor topologies, ten-switch structure faces restriction on its allowable switching states for the shared leg. Table I and II reflects various switching states for the twelve and ten-switch configurations, respectively. It can be clearly seen from Table II that the output terminals for the shared leg "C" can be connected to either Vdc or ground. Unlike the back-to-back configuration, the switching state where the upper terminal is connected to Vdc and lower terminal is connected to ground (i.e. Vsh = Vdc and Vsr = 0) or vice-versa is not realizable as it will result in a direct short circuit of the dc bus. The blocking of two (out of four) states limits the dc link voltage available for the shared leg ("phase C") to half of its value for back-to-back configuration.

TABLE.1 SWITCHING STATES IN TWELVE-SWITCH CONFIGURATION

VOLTAGE	SWITCHING STATES
$V_{sh} = V_{sr} = V_{dc}$	S_{C1} , $S_{C1}{'}$ = ON and S_{C2} , $S_{C2}{'}$ = OFF
$V_{sh} = V_{sr} = 0$	S_{C2} , $S_{C2}{'}$ = ON and S_{C1} , $S_{C1}{'}$ = OFF
$V_{sh} = V_{dc}$ and $V_{sr} = 0$	S_{C1} , $S_{C2}{'}$ = ON and S_{C2} , $S_{C1}{'}$ = OFF

TABLE.2 SWITCHING STATUS FOR TEN SWITCH CONFIGURATION

VOLTAGE	SWITCHING STATES
$V_{sh} = V_{sr} = V_{dc}$	S_{C1} = ON and S_{C2} = OFF
$V_{sh} = V_{sr} = 0$	S_{C1} = OFF and S_{C2} = ON
$V_{sh} = V_{dc}$ and $V_{sr} = 0$	NOT REALIZABLE
$V_{sh} = 0$ and $V_{sr} = V_{dc}$	NOT REALIZABLE

Ten-switch configuration was earlier reported in to replace twelve-switch back-to-back converter for dual induction machine drive system. Although the arrangement allows independent control of both machines with a wide range of variation in load torque and rotational speeds, it imposes restrictions on the dc link voltage. If Um1and Um2 are the maximum values of phase-to- phase voltages at the junctions of the induction machine M1 and M2 , respectively, it is shown that,

$$VDC \geqslant max(Um1 + Um2) \text{ for ten switch system.} \qquad (1)$$
$$VDC \geqslant max(Um1 , Um2) \text{ for twelve switch system.} \qquad (2)$$

Where VDC is the voltage across the dc link capacitor. In the special case of Um1= Um2 =U the following constraints can be established.

$$VDC \geqslant 2U \text{ for ten switch system.} \qquad (3)$$
$$VDC \geqslant U \text{ for twelve switch ststem.} \qquad (4)$$

Equation 3 and 4 implies that the dc link voltage must be doubled to achieve the maximum rotational speed for both machines simultaneously. Doubling of dc link voltage increases all the component stress by two folds, thus, offsetting the saving of two switches. For the same dc link voltage, the ten-switch structure leads to reduction in the terminal voltage and consequent speed range of both machines.

Attempts to enhance the dc-bus utilization for the ten-switch architecture have been reported. The improvement reported, is obtained at the expense of identical operating (speeding and loading) conditions for both machines. In the controller divides the dc link voltage by allocating predefined switching vectors to each machine. The restriction that the controller must have prior knowledge of the voltage profile for each machine makes the scheme impractical for variable industrial loads. The ten-switch configuration is employed to drive the two induction motors in the center driven winders. It overcomes the limitation of dc link over sizing given by 'inverse loading profile" of the two machines. When one motor operates at maximum speed, the other motor operates at minimum speed and vice versa. Since both motors increase/decrease speed in an alternate fashion, their voltage requirement is completely different (opposite). This allows the ten-switch system to remain operational for center driven winders utilizing the same dc link voltage required for back-to-back converter. However, the center driven winder is a special case and in general ten-switch configuration have not shown much economic value for dual motor drive systems.

Proposed work

This paper proposes the use of ten-switch configuration as the most suitable candidate for shunt-series configuration, such as, UPQC. The rationale behind this recommendation is given below. The outputs of the upper VSI are connected to the PCC constituting the shunt configuration, whereas, the outputs of lower VSI are connected in series with the same PCC constituting the series configuration. The shared set of switches Sc1 and Sc2 are driven by the modulation signal which is calculated as follows.

$$mres = msh + msr \qquad (5)$$

Where and are the amplitude of the modulating signal for shunt and series VSIs, respectively. is the resultant modulating signal for the shared set of switches. To maintain the linear range of modulation for and the maximum allowable limit for is -1 to +1.Thus, up to 15% THD in the PCC voltage can be compensated without increasing the dc-link voltage. For higher values of voltage THD, like all existing configurations, the proposed topology will also require a higher dc-link voltage.

During normal condition, the shunt VSI supplies harmonic and fundamental reactive component of the load current while the series VSI injects the inverse of PCC voltage harmonics usually < 5% [11]. Since the shunt VSI operates at the same voltage level as PCC (1 p.u.), its reference signal amplitude is also unity. The amplitude of the reference signal for shared leg can go as high as 1.05. If an ideal grid is considered (with no distortion in PCC voltage) the series VSI will simply operate with a modulation index of zero and.

Now consider that there is sag of magnitude V in the PCC voltage. On the occurrence of sag, the PCC voltage undergoes a reduction of V. The shunt VSI modulation index also decreases proportionally to the new value of V. Where V is the nominal load voltage. It can be observed from Figures that the resultant modulation signal for the shared leg (phase "C") does not extend out of the dc-link bandwidth during both (normal and sag) modes of operation. This is attributed to the fact that amplification in by any amount is always accompanied by a reduction in by the same factor. The self-tuning feature of both the modulation references causes the shared leg switches to always operate in the linear range of modulation. Thus, the proposal of the utilization of a ten-switch topology for UPQC can be concluded as the most suitable application.

IV. RESULT AND DISCUSSION

The simulation output for the power quality improvement is estimated by using ten switch inverter model. The output waveforms are experimented with and without using UPQC in the block diagram.
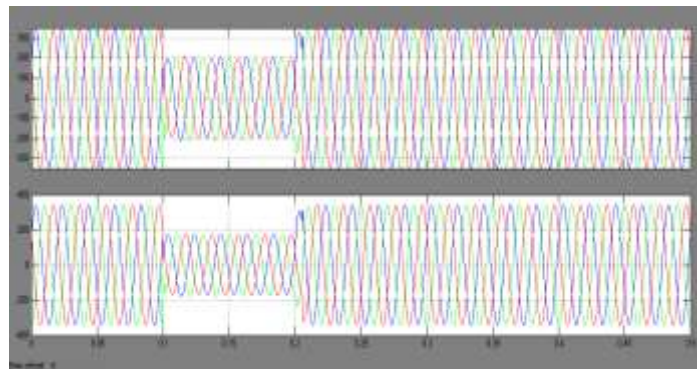

Figure 4.1 simulation output voltage waveform without using UPQC

In the above figure it is found that the output voltage waveform is distorted due to the fluctuations in the voltage during without using UPQC.
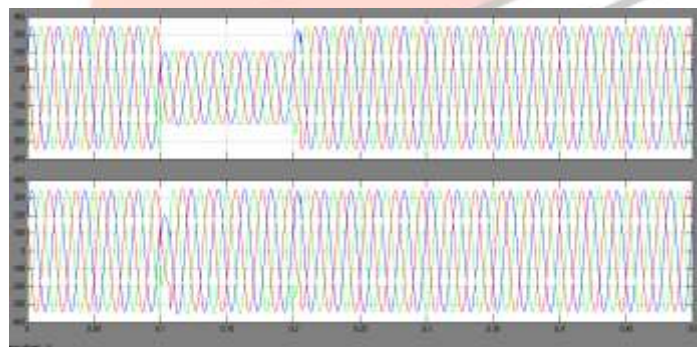

Figure 4.2 Simulation output voltage waveform with using UPQC

In the above figure it is found that the voltage fluctuations is removed and uniform voltage is received at the output during UPQC is installed. The total harmonic distortion in the voltage waveforms with and without using UPQC is plotted below.
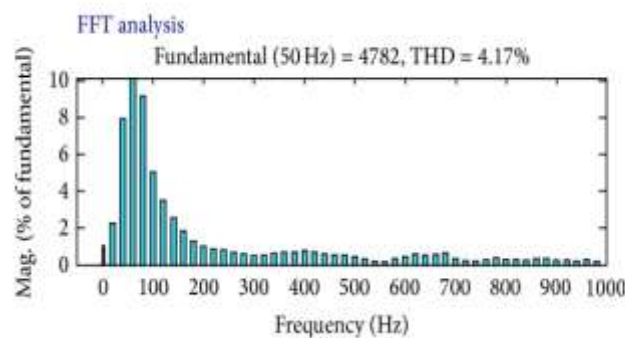
Figure 4.3 Total harmonic distortion waveform without using UPQC

In the above figure the total harmonic distortion for the fundamental frequency is found to be high during without using UPQC. Similarly, the THD for the fundamental frequency (50Hz) is considerably less (0.49%) during UPQC is used. While UPQC is used the voltage waveform is not fluctuated and found to be uniform for the given period of time. The quality of the power is usually determined by the percentage of distortion is seemed during the normal frequency range of 50Hz. By installing UPQC the major issues in the power quality is reduced and the stable and sustained power is obtained in the entire arrangement of the power structure. In the above figure it is found that the THD is reduced by using UPQC during the fundamental frequency range.
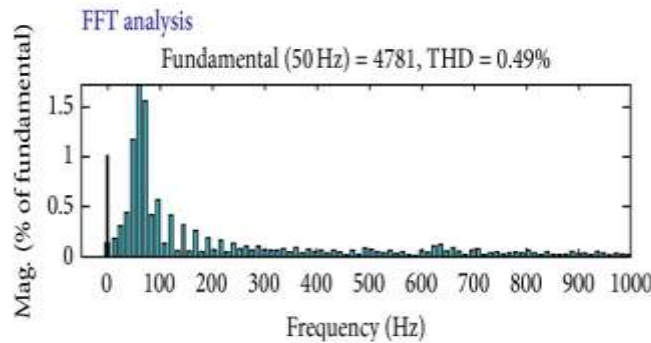
Figure 4.4 Total harmonic distortion waveform with using UPQC

V. CONCLUSIONS

To overcome the limitations of twelve- switch based power conditioner, this project proposes a new structure of UPQC using ten semiconductor switches. The salient features of the proposed topology are its capability of maintaining the same power quality enhancement with less number of switches and without increasing the switch VA rating. A comparative study is conducted and the results demonstrate that the proposed ten switch topology can achieve the same power quality mitigation performance with the least VA loading of the UPQC system. The performance of the proposed topology has been validated experimentally under various operating conditions. The UPQC performs principally depends upon however accurately and quickly reference signals are derived. The simulation results have shown that the UPQC perform higher with FLC planned them eliminates each voltage and current harmonics effectively. The proposed model for the ten switch UPQC is to compensate input current harmonics and voltage harmonics caused by non-linear loads. Fuzzy learning algorithm used in power quality improvement lags in speed response and stability. In order to overcome these drawbacks, Neuro-fuzzy logic algorithm can be used in the future work. And more over the number of switches in the topology structure can also be reduced.

REFERENCES

[1] Hideaki Fujita, Hirofumi Akagi, (1998)"The unified power quality conditioner: The Integration of Series and Shunt-Active filters", IEEE Transaction on Power Electronics, Vol. 13, no. 2, pp. 315- 322.

[2] P. Delarue, A. Bouscayrol and E. Semail, (2003)"Generic control method of multileg – voltage source converter for practical implementation", IEEE Transaction on Power Electronics, Vol. 18, no.2, pp. 517- 526

[3] Yunevei Li, D. Mahinda Vilanthgamunva, (2005)"Microgrid Power Quality enhancement using a Three- Phase Four-wire Grid Interfacing compensator", IEEE Transaction on Industry Application, Vol. 41, no. 6, pp. 1707-1719

[4] B. Han, B.Kim and S. Back, (2006)"Combined operation of Unified Power Quality Conditioner with Distributed generation", IEEE Transaction on Power Delivery, vol. 21, no. 1, pp. 330- 338

[5] M. Jones, D. Dujic, E. Levi, M. Bebic and B. Jefteni, (2007)"A two motor centre driven winder fed by a five- leg Voltage source inverter", Proc. Eur. Conf. Power Electronics, pp. 1-10.

[6] Hamid Reza Mohammadi, Ali Yazdiam varjani, Hassein Mokhtari, (2009)"Multiconverter Unified Power Quality conditioning system: MC – UPQC", IEEE Transaction on Power Delivery, Vol. 24, no. 3, pp. 1679- 1686.

[7] Vinod Khadkikar, Amblish Chandra, (2009)"A novel structure for Three- Phase Four- Wire Distribution system", IEEE Transaction on Industrial Application, Vol. 45, no. 5, pp. 1897- 1902

[8] Vinod Khadkikar, Amblish Chandra, (2009)"A novel concept of simultaneous voltage sag/ swell and load reactive power compensations utilizing series inverter of UPQC", IEEE Transaction on Power Electronics, Vol. 26, no. 9, pp. 2414- 2425

[9] M. Venkateswarlu, Samual George, (2013)"A novel control method for Unified Power Quality conditioner using nine-switch power conditioner", International Journal of Engineering Trends and Technology, Vol. 4, no.6.

[10] Vinod Khadkikar, (2016)"Enhancing electric Power Quality using UPQC: A comprehensive overview", IEEE Transactions on Power Electronics, Vol. 27, no.5, pp. 2284- 2297.